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CMOS fabrication for scalable trapped-ion quantum information processing

Master Thesis

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Abstract

This thesis describes the design, fabrication, and testing of a surface-electrode trap (SET) fabricated in commercial complementary metal-oxide-semiconductor (CMOS) foundry. To reduce the curvature of the radio frequency (RF) potential along the axial direction, the shape of the RF electrodes on this SET has been optimized. The multi-layer structure from the CMOS technology has been made use of to route the tracks in a layer underneath the electrodes, which grants us more flexibility in patterning the electrodes, helps us reduce the size of the chip, and makes it possible to realize the round end-caps on the RF electrodes. To mill the backside-loading slot onto this trap, which avoids the contamination of the trap surface by the atomic flux during the trap loading, several possible technologies have been studied and compared, and eventually focused ion beam (FIB) was selected. Testing runs of the FIB have been done to search for the best milling strategy, and chip holders have been designed specifically for our milling strategy, to protect the trap surface from contamination and scratching during the milling process.

In addition, some surrounding electronics have been built for this trap. A quarter-wave helical resonator which fits our cryostat is designed and built to provide the necessary RF voltage at 40 MHz. An RF-pickup circuit is realized which uses a transistor to avoid the noises injecting into the experimental system, and uses a 1 pF capacitor as its front end so that it will minimally affect the other parts of the system. This circuit can be used to monitor the RF voltage on the trap in real time in our future experiments. In order to find a digital-analog-converter (DAC) working at 4 K, so that the cumbersome through-vacuum feedthroughs connecting the DACs to the trap can be saved, the cryo-compatibility of DACs from several manufacturers have been tested, but unfortunately no working one has been found yet.

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Contents

Chapter 1

Introduction

Trapped atomic ions have proved to be a promising candidate for quantum information processing, as all the DiVincenzo criteria for a quantum computer [1, 2], which include:

- A well-defined two-level system as the quantum bit (qubit),
- The ability to reliably initialize the quantum state,
- Long enough coherence time of the qubits comparing to the gate times of the quantum operations,
- The realization of a set of universal quantum gates,
- The ability to measure out the states of the qubits,

have been fulfilled [3] and high-fidelity quantum operations have been demonstrated [4]. To fully exploit the power of the trapped-ion quantum computing, and to overpower the classical computers eventually, scaling up the trapped-ion systems to large number of qubits is now of essential importance.

Two schemes to scale up the trapped-ion systems have been proposed: the quantum charge-coupled device (QCCD) architecture [5], and the 2D array of microtraps [6]. The QCCD architecture consists of a large number of interconnected ion traps, which are defined as memory regions and interaction regions. The quantum information carriers – the ions, are stored in the memory regions. When quantum logic gates are needed, the relevant ions are transported to the interaction region, where the lasers are focused to drive the gates. After the operation is done, the ions are moved back to the memory regions. In the 2D microtrap array approach, single ions are loaded to independent microtraps, and a different ion (Head) can move above them, approaching any particular ion. Single-qubit operations can be directly done by addressing the laser to the individual ions. Two-qubit gates are realized

with the help of the Head, which first interacts with one target ion, then moves to the other target trapped in another microtrap, and interacts with it.

To scale up the trapped-ion system with the QCCD architecture, surface-electrode traps (SETs), where the electrodes are planarized and all placed on a single plane, have been proposed and realized [7, 8, 9, 10]. This structure is more straightforward for fabrications, making it easier to be scalable in both senses, the number of electrodes and the realization of trap arrays. Since such SET structure is compatible with the very large scale integrated-circuit (VLSI) technologies originally developed for the semiconductor industry [8, 11], it is a promising solution for the 2D microtrap array approach as well, as in principle hundreds or thousands of microtraps can be built on a single chip using the VLSI technologies [12]. Recently, a surface electrode trap was fabricated using the commercial CMOS (complementary metal-oxide-semiconductor) foundry process [13], which for the first time introduced industry standard fabrication processes to the realizations of scalable quantum processing systems.

CMOS is a well-established technology already widely used in the semiconductor industry. It has proved to be scalable in building the VLSIs. The metal layers originally used for the interconnection of MOS transistors is also suitable to form the surface-electrodes of our ion trap. This gives us the opportunity to use this scalable fabrication process to scale up our trapped-ion systems. Besides this advantage, decades of developments have reduced the linewidth of the CMOS technology to only tens of nanometers. This allows tiny structures (comparing to the length scale of typical ion traps) to be built on the traps, and allows the high-precision fabrication of miniaturized ion traps. The multiple layers in the CMOS structure grant us more freedom in the designing of the traps than the conventional single-layer structure, like placing tracks underneath the trap and placing multiple ground planes. By sharing the masks and wafers with other customers, the cost for the CMOS fabrication (about 8000 Euros for 50 samples in our case) is lower than the specialized, nonstandard trap fabrications in cleanrooms, and its yield is higher. Originally developed for the integrated circuits (ICs), and benefited from the popular research in Si-based photonics in the recent one to two decades (a recent review of the status of this field can be found in [14]), CMOS technology also opens the door to integrating electronics and photonics to the ion traps.

Inspired by the promising future of the CMOS fabricated SETs, I have designed our own CMOS SET and had it fabricated in a commercial CMOS foundry. In my design, I optimized the shape of the radio frequency (RF) electrodes to minimize the RF potential curvature along the axial direction, so as to reduce the ion's micromotion when transported axially. Making

use of the multiple metal layers, I routed the tracks which connect the wirebonding pads to the corresponding electrodes, in an interconnection layer below the trap electrodes. This provides us more flexibility in the placement of the electrodes, and makes the realization of the optimized round endcaps on the RF electrodes possible, which otherwise have to be replaced by the RF tracks. This improvement also makes it possible to introduce spatially isolated 'island' electrodes to the SET, which otherwise can hardly be electronically connected to the wirebonding pads. Furthermore, routing underneath the trap surface saves us spaces in the top metal layer, which therefore reduces the chip size.

To minimize the contamination on the trap surface by the neutral atomic flux when loading ions to the trap, we decided to cut a backside-loading slot on this trap. To find the proper method for this task, I have studied and compared several possible milling/etching solutions, and eventually determined to use the focused ion beam (FIB), because of its material compatibility and fast milling rate. Test runs of the FIB have been done to find the best milling strategy for our chip.

One drawback of the SETs is the reduced pseudo-potential depth, which makes the ions easier to lose and ion chains easier to reorder due to collisions with background gas [15]. Besides, since the ion-electrode distances are typically smaller in the miniaturized traps, the ions will be more influenced by the anomalous heating effect [16]. To lower the background pressure and to reduce the heating rates, our SET is operated in a cryostat. The cryogenic temperature also relaxes the requirements for ultra-high vacuum (UHV) compatible electronics, because the outgassing of materials is significantly reduced at such temperature.

However, the use of cryostat poses problems in feeding the necessary high RF voltages to the trap, because of the Joule dissipation and the noise pickup on the long in-vacuum cables. The solution is to send only small amount of RF power from outside the cryostat, and to use a resonator to amplify the RF voltage inside the cryostat. A resonator with high quality value (Q value) will also filter out the noises on the RF waveform. For this reason, I designed and built a coaxial helical quarter-wave RF resonator for the RF frequency of the new SET, which fits our cryostat.

As the trap scales up, there will be more DC electrodes requiring DC voltage inputs. One scalable solution to the increasing demand of DC voltages is using multi-channel digital-analog-converters (DACs). However, to connect the output channels of the DACs to the ion trap operated in the cryostat, through-vacuum feedthroughs and long cables must also be used. These cables are cumbersome, which eventually will limit the scaling up of the ion traps. Moreover, it's likely that noises are picked-up on these long cables as well. If we can place the DACs also into the cryostat, the requirement for

those feedthroughs and cables can be saved, and the whole system is greatly simplified. For this reason, I have tested various DACs to check their cryo-compatibility, attempting to find a working DAC at 4K environment, but I didn't unfortunately.

To monitor the RF voltage applied to the trap, I designed and realized an RF-pickup circuit, which uses a field emission transistor (FET) to avoid noise from the measurement apparatus and the feedthrough injecting into the trap, while allows the attenuated RF signal going outside the experimental setup to be measured. To minimize the influence of this circuit to the other parts of the system, like the matched impedance for the RF resonator loaded with the trap, and the resonant frequency and Q value of the resonator, I used a 1 pF capacitance as the frontend of this RF pick-up circuit.

In this thesis, I will first briefly review the physics for ion trapping and the basic structures of SET in Chap. 2. Then I will discuss the design and the layouts of this trap, respectively in Chap. 3 and Chap. 4. In Chap. 5, I will review the several etching/milling methods for making the backside loading slot, and discuss the practices in milling with FIB. Chap. 6 deals with the surrounding electronics for this trap, including the RF resonator, the RF-pickup circuit, and the cryo-compatibility tests for DACs. In Chap. 7 I present the results of the measurements I have done to characterize this new trap. The thesis ends up with Chap. 8 as an outlook.

Chapter 2

RF Paul ion trap

Ion-trapping is the art of suspending charged particles in vacuum, by confining their motions with electromagnetic fields. Since the trapped ions are well isolated from the environment, they can be cooled to motional ground state by laser cooling, and their motional spectrum is relatively simple. Both their internal electronic states and external motional states can be coupled and manipulated with laser fields [17, 18]. This makes them a good candidate for quantum information processing.

For quantum information processing, RF Paul traps are most used, which confine the motions of ions with a combination of RF and DC fields. The new trap we designed and fabricated in this work is also based on the Paul trap scheme. Therefore in this chapter I will give an overview of the theory for ion-trapping, especially the RF Paul trap, and then discuss the geometry of SET.

2.1 RF Paul trap

Their are two approaches to understand the physics of RF Paul trap, i.e. the fully detailed Mathieu equation treatment, and an easier treatment based on a pseudo-potential approximation. The Mathieu equation treatment fully solves the ion's equation of motion under the time-varying and periodic electrical potential. While under the assumption that the amplitude of the fast oscillation is much smaller than the slow oscillation (the pseudo-potential condition), we can treat the RF field as an effective ponderomotive potential. The former treatment gives us the insight about the ion's micromotions (the fast oscillations with small amplitudes) in the trap, while the latter one is handy when seeking for the proper parameters of the new trap by doing simulation. In this section I will first go through the Mathieu equation treatment, and then discuss the pseudo-potential approximation.

2.1.1 Mathieu equation treatment

In order to trap charged particles, we can make use of the electromagnetic fields. However, as a consequence of the Laplace condition for electrostatic potentials in free space,

$$\triangle\Phi = \frac{\partial^2\Phi}{\partial x^2} + \frac{\partial^2\Phi}{\partial y^2} + \frac{\partial^2\Phi}{\partial z^2} = 0, \tag{2.1}$$

electrostatic potentials cannot be confining in all three directions. To trap ions, either a static magnetic field (Penning trap) or a time-variant electric field (Paul trap) is used to confine the ions in two directions, while a static electric field provides confinement along the third direction [18].

For a Paul trap, the electric potential near the trap minimum, whose coordinate is denoted as (0,0,0), can be expanded to second order as

$$\Phi(x_1, x_2, x_3, t) = \frac{1}{2}\sum_{i=1,2,3}[u_i + v_i\cos(\Omega_{\mathrm{RF}}t)]x_i^2 \tag{2.2}$$

where u_i and v_i are the curvatures along the i-direction created by the DC and the RF voltages respectively, x_i are the coordinates on the i-th principal axis for the trap, which happen to be the Cartesian coordinates for a non-rotated symmetric trap [1], and Ω_{RF} is the angular frequency of the RF field. Here the 0-th order term is ignored because it can be eliminated by redefining the potential zero, and so are the 1-st order terms because they are only a shift of the potential minimum, which can be absorbed into the quadratic terms and therefore be eliminated by defining the trap minimum position as (0,0,0). Higher order terms will in principle also appear in Eq. 2.2, however, when the ions are confined in a region small enough, these terms are negligible. For laser cooled ions confined in a Paul trap, this is usually a good approximation.

Plugging Eq. 2.2 into the equation of motion of the ion, we get

$$\frac{\mathrm{d}^2x_i}{\mathrm{d}t^2} = -\frac{Q}{m}\frac{\partial\Phi}{\partial x_i} = -\frac{Q}{m}[u_i + v_i\cos(\Omega_{\mathrm{RF}}t)]x_i, \tag{2.3}$$

where Q and m are the charge and mass of the ion respectively. Substituting into Eq. 2.3 the dimensionless variables

$$\tau = \frac{\Omega_{\mathrm{RF}}t}{2}, a_i = \frac{4Qu_i}{m\Omega_{\mathrm{RF}}^2}, q_i = \frac{2Qv_i}{m\Omega_{\mathrm{RF}}^2}, \tag{2.4}$$

[1] The more general form of this equation, when the Cartesian axes are not the principal axes for the system, writes $\Phi(x_1, x_2, x_3, t) = \frac{1}{2}\sum_{i,j=1,2,3}[u_{ij} + v_{ij}\cos(\Omega_{\mathrm{RF}}t)x_ix_j]$, where non-diagonal elements of the Hessian come into play, and the Mathieu equations for the three Cartesian coordinates as will be derived later get coupled with each other.

the equation of motion Eq. 2.3 can be written as

$$\frac{\mathrm{d}^2 x_i}{\mathrm{d}\tau^2} + [a_i + 2q_i \cos(2\tau)]x_i = 0, \tag{2.5}$$

which has the form of a Mathieu equation. For a linear Paul trap, ideally the RF curvature is non-zero only in the $i = 2, 3$ directions, while in the $i = 1$ direction there is only the DC curvature, so we have $q_1 = 0$ correspondingly.

The general solutions to the Mathieu equation are given by Floquet's theorem [17, 18, 19]

$$x_i(\tau) = A_i e^{\mu_i \tau} \sum_{n=-\infty}^{\infty} C_{2n,i} e^{j2n\tau} + B_i e^{-\mu_i \tau} \sum_{n=-\infty}^{\infty} C_{2n,i} e^{-j2n\tau}, \tag{2.6}$$

where μ_i and C_{2n} depend purely on a_i and q_i, while A_i and B_i are constants determined by the initial conditions.

If μ_i has a non-zero real part, we will have $x_i \to \infty$ when $\tau \to \infty$. So for the solution to be stable, μ_i has to be purely imaginary ($\mu_i \equiv i\beta_i$).

By plugging Eq. 2.6 back into Eq. 2.5 we get the relation for the coefficients C_{2n}:

$$-D_{2n,i}C_{2n,i} + (C_{2n+2,i} + C_{2n-2,i}) = 0, \tag{2.7}$$

where $D_{2n,i}$ is defined as $D_{2n,i} \equiv [a_i - (\beta_i + 2n)^2]/q_i$.

By recursively using Eq. 2.7 we can get the expressions for $C_{2n,i}$

$$\frac{C_{2n,i}}{C_{2n-2,i}} = \frac{1}{D_{2n,i} - \frac{C_{2n+2,i}}{C_{2n,i}}} = \frac{1}{D_{2n,i} - \frac{1}{D_{2n+2,i} - \frac{C_{2n+4,i}}{C_{2n+2,i}}}} = \frac{1}{D_{2n,i} - \frac{1}{D_{2n+2,i} - \frac{1}{D_{2n+4,i} - \frac{1}{\cdots}}}}, \tag{2.8}$$

and

$$\frac{C_{2n,i}}{C_{2n+2,i}} = \frac{1}{D_{2n,i} - \frac{1}{D_{2n-2,i} - \frac{1}{\cdots}}}. \tag{2.9}$$

Letting $n = 0$ in Eq. 2.7, then recursively using Eq. 2.8 and Eq. 2.9, we get an expression for β_i with continued fractions:

$$\begin{aligned}
\beta_i^2 &= a_i - q_i D_0 = a_i - q_i\left(\frac{C_2}{C_0} + \frac{C_{-2}}{C_0}\right) \\
&= a_i - q_i\left(\frac{1}{D_{2,i} - \frac{1}{D_{4,i} - \frac{1}{\cdots}}} + \frac{1}{D_{-2,i} - \frac{1}{D_{-4,i} - \frac{1}{\cdots}}}\right) \\
&= a_i + \frac{q_i^2}{(\beta_i + 2)^2 - a_i - \frac{q_i^2}{(\beta_i+4)^2 - a_i - \ldots}} + \frac{q_i^2}{(\beta_i - 2)^2 - a_i - \frac{q_i^2}{(\beta_i-4)^2 - a_i - \ldots}}.
\end{aligned} \tag{2.10}$$

Typically, Paul traps are operated under the so-called pseudo-potential condition [17, 18]

$$|a_i| < q_i^2 \ll 1, \tag{2.11}$$

such that β_i can be approximated as [2]

$$\beta_i^2 \approx a_i + \frac{q_i^2}{2} \tag{2.12}$$

and the coefficients $C_{\pm 2n}$ decrease rapidly as n increases. Therefore terms with $n > 1$ can be neglected. And under the initial condition $A_i = B_i$, Eq. 2.6 can be simplified as

$$x_i(t) \approx 2A_iC_{0,i}[1 - \frac{q_i}{2}\cos(\Omega_{\mathrm{RF}}t)]cos(\beta_i\frac{\Omega_{\mathrm{RF}}t}{2}) \tag{2.13}$$

This trajectory can be interpreted as a harmonic oscillation with secular frequency $\omega_i = \beta_i\frac{\Omega_{RF}}{2}$, whose amplitude is modulated at the RF frequency Ω_{RF}. The superimposed high frequency component onto the secular motion is called *micromotion*, as its amplitude is $\frac{q_i}{2}$ times smaller than the amplitude of the secular motion.

2.1.2 Pseudo-potential approximation

A simpler treatment of the ion's motion than the fully detailed Mathieu equation approach is doing the pseudo-potential approximation. As a result, the RF field is effectively approximated as a static field, the so-called pseudo-potential. This approach deals with the RF field alone, and intuitively shows purely its influence on the ion's motion. This is very helpful for the simulation work that will be discussed in the next chapter.

Within this approach, the ion's motion $x_i(t)$ is split into a slowly-oscillating component $X_i(t)$ plus a fast-oscillating component $\varepsilon_i(t)$

$$x_i(t) = X_i(t) + \varepsilon_i(t), \tag{2.14}$$

and the amplitude of the fast-oscillating component is assumed to be much smaller than the slowly-oscillating component, $\Delta\varepsilon_i^2 \ll \Delta X_i^2$. If the pseudo-potential condition Eq. 2.11 as discussed in the previous section is fulfilled, this assumption holds as well.

Expanding the RF field to first order in space, we get[3]

$$E_{\Omega,i}(x_i, t) = E_{\Omega,i}(x_i)\cos(\Omega_{\mathrm{RF}}t) = [E_{\Omega,i}(X_i) + \varepsilon_i\frac{\mathrm{d}E_{\Omega,i}(X_i)}{\mathrm{d}x}]\cos(\Omega_{\mathrm{RF}}t). \tag{2.15}$$

[2] First, all the a_i and q_i^2 terms in the denominator can be neglected, as they must be much smaller than $(\beta_i \pm 2)^2 > 4$, therefore $\beta_i^2 \approx a_i + \frac{2q_i^2}{(\beta_i+2)^2}$. From this we can readily conclude that $\beta_i^2 \ll 1$ so that the β_i appearing in the denominator can also be neglected, and then we get $\beta_i^2 \approx a_i + \frac{q_i^2}{2}$.

The ion's equation of motion under this RF field therefore writes

$$\frac{\mathrm{d}^2 x_i}{\mathrm{d}t^2} = \frac{\mathrm{d}^2 X_i}{\mathrm{d}t^2} + \frac{\mathrm{d}^2 \varepsilon_i}{\mathrm{d}t^2} = \frac{Q}{m}[E_{\Omega,i}(X_i)\cos(\Omega_{\mathrm{RF}}t) + \varepsilon_i \frac{\mathrm{d}E_{\Omega,i}(X_i)}{\mathrm{d}x}\cos(\Omega_{\mathrm{RF}}t)]. \tag{2.16}$$

Note that the slowly-oscillating term $\frac{d^2X}{dt^2}$ only arises from the inhomogeneity of the oscillating field[4], and under the assumption that $\Delta\varepsilon_i^2 \ll \Delta X_i^2$, the small fast-oscillating motion is essentially determined only by the field strength at position X_i. Therefore Eq. 2.16 can be separated into two equations, which we require to be fulfilled simultaneously

$$\frac{d^2\varepsilon_i}{dt^2} = \frac{Q}{m}E_{\Omega,i}(X_i)cos(\Omega_{RF}t), \tag{2.17}$$

$$\frac{d^2X_i}{dt^2} = \frac{Q}{m}\varepsilon_i\frac{dE_{\Omega,i}(X_i)}{dx}cos(\Omega_{RF}t). \tag{2.18}$$

Eq. 2.17 gives us

$$\varepsilon_i = -\frac{Q}{m\Omega_{\mathrm{RF}}^2}E_{\Omega,i}(X_i)\cos(\Omega_{\mathrm{RF}}t). \tag{2.19}$$

Substituting Eq. 2.19 into Eq. 2.18 and averaging over one oscillation period of the RF field, we get

$$\begin{aligned}\langle\frac{\mathrm{d}^2X_i}{\mathrm{d}t^2}\rangle_{\mathrm{RF}} &= -\frac{Q^2}{m^2\Omega_{\mathrm{RF}}^2}\langle E_{\Omega,i}(X_i)\frac{\mathrm{d}E_{\Omega,i}(X_i)}{\mathrm{d}x}\cos^2(\Omega_{\mathrm{RF}}t)\rangle_{\mathrm{RF}} \\ &= -\frac{Q^2}{4m^2\Omega_{\mathrm{RF}}^2}\frac{\mathrm{d}}{\mathrm{d}x}E_{\Omega,i}^2(X_i).\end{aligned} \tag{2.20}$$

Using the ansatz

$$\frac{\mathrm{d}^2x_i}{\mathrm{d}t^2} = -\frac{Q}{m}\frac{\mathrm{d}U_{eff,i}}{\mathrm{d}x_i}, \tag{2.21}$$

we end up with the effective pseudo-potential which determines the secular motion

$$U_{eff,i} = \frac{Q}{4m\Omega_{\mathrm{RF}}^2}E_{\Omega,i}^2(X_i). \tag{2.22}$$

In the simulation which will be discussed in the following chapter, this relation is used to model the influence of RF field on the ion's motion.

By substituting $E_{\Omega,i}(X_i) = v_iX_i$ into Eq. 2.20, where v_i is the curvature of RF potential along i-th direction as defined in the previous section, we get

$$\langle\frac{\mathrm{d}^2X_i}{\mathrm{d}t^2}\rangle_{\mathrm{RF}} = -\frac{Q^2}{2m^2\Omega_{\mathrm{RF}}^2}v_i^2X_i. \tag{2.23}$$

[3]For simplicity, the time-dependence in $x_i(t)$, $X_i(t)$ and $\varepsilon_i(t)$ is left out.

[4]In the extreme limit, consider the motion of the ion under a spatially homogeneous field ($\frac{dE_{\Omega,i}}{dx} = 0$). The ion will only undergo the fast oscillation, but the center of its oscillation will never shift ($\frac{dX_i}{dt} = 0$).

Therefore the secular frequency is

$$\omega_i = \frac{Q}{\sqrt{2}m\Omega_{\mathrm{RF}}} v_i. \tag{2.24}$$

We can easily verify that this secular frequency derived from pseudo-potential is identical to the secular frequency $\omega_i = \beta_i \frac{\Omega_{\mathrm{RF}}}{2}$ solved from Mathieu equation in the previous section, if we put $a_i = 0$ and plug the definition of q_i in Eq. 2.4 into it.

2.2 Surface-Electrode trap

SETs are one type of realization of the RF Paul trap, whose theory of operation fully follows the discussions in the previous section. On a SET, all the electrodes are planarize, and placed in the same surface. Compared to the 4-rod trap [20, 21], and the wafer trap [22], SETs have the advantages that they are easier to fabricate, and can be scaled up by making use of the well-established semiconductor technologies developed for VLSI [8, 11].

The 5-wire trap (Fig. 2.1) is so far the most commonly used type of SET [8, 9, 13]. The innermost one and the outermost two electrodes are RF grounded and DC biased, while the rest two are connected to the RF drive. Such a geometry can be understood as a 4-rod trap, one of whose two DC rods is split into two parts, and the resulted 5 rods are re-patterned into a single surface. To gain more control over the ion's motion and position, and make it possible for ion transportation, the outermost two DC electrodes are segmented, therefore different DC voltages can be applied to them.

Fig. 2.2 shows the pseudo-potential created by a 5-wire SET, in the $y - z$ plane. Since all the electrodes for the SET are placed in the $x - y$ plane, SETs suffer from the much shallower trap depth in z-direction comparing to the 3D traps, which makes the ions easier to lose, and the ion chains easier to reorder, due to the collisions with background gas. For this reason, our experiments with SET are done in the cryogenic environment, where the background pressure is lowered, and the heating from the trap is reduced. This improves the ion lifetime in the trap. Also, since outgassing is greatly reduced in cryogenic temperature, normal electronic chips and PCBs are allowed to be used, which do not have to be UHV compatible.

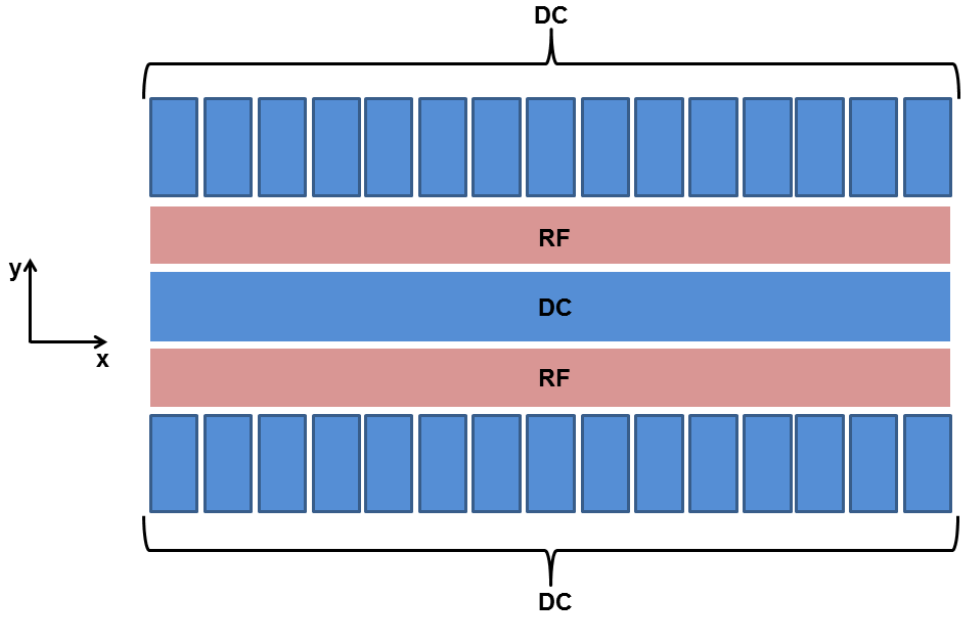


Figure 2.1: Example of a 5-wire surface electrode trap. RF voltage is applied to the 2nd and 4th 'wires', and the outermost (1st and 5th) DC electrodes are segmented for more flexible control over the ion's position and axial motion.

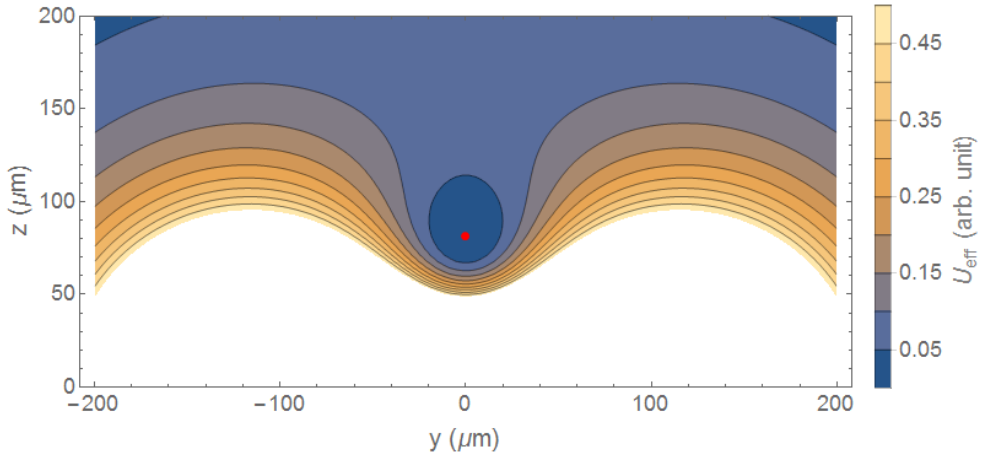


Figure 2.2: Pseudo-potential generated by a symmetric 5-wire surface trap. The lighter the color, the higher the potential. Pseudo-potential minimum is shown as the red dot. For clarity, contours for pseudo-potential values above 0.5 A.U. are not shown.

Chapter 3

Trap design

To design the trap, first I have done a simulation to fix the dimensions of the electrodes according to our requirements for this trap, such as the ion-electrode distance and the trapping frequencies. During the simulation process, a round end-cap of the RF electrodes was found to be able to reduce the axial curvature of the pseudo-potential, which can be helpful for the ion transportation experiments. The shape of this round structure is thereafter optimized.

In this chapter, the simulation method is briefly reviewed and then the dimensions we decided for the new trap are shown. Afterwards, I will discuss the round RF cap structure, and the optimization method for determining it. In the last part of this chapter, the key parameters and features of this trap are summarized.

3.1 Simulation

Some properties of the trap purely depend on the trap geometry, for example the height of RF minimum in a 5-wire configuration depends only on the widths of the two RF electrodes and the central electrode, and the width of the segmented DC electrodes affects the DC voltage needed to provide the necessary axial confinement. These dependencies provide the very first starting point for the trap design. With the help of the simulation, these geometric parameters can be iterated, to shoot for the desired trap properties.

The simulation was based on the SurfacePattern software package written by Romand Schmied [23, 24, 25] and extended by Felix Krauth [26]. In this package the electrostatic potential and its spatial derivatives up to 5th order, generated by a finite electrode of the given shape, for unity input voltage, are analytically solved. A useful way to define the shapes of the electrodes in this software is to describe them as polygons, where the coordinates of

all the vertices are given as input. In this way, essentially arbitrary shapes, such as round segment, can be approached just by increasing the number of vertices of the polygon. According to the superposition law for electric potentials, we can calculate the potential for each of the electrode on the trap separately, and sum them up with the corresponding coefficients to get the overall potential generated by the whole trap.

The pseudo-potential providing radial confinement is calculated from the RF electric field strength, according to Eq. 2.22. The spatial derivatives of this pseudo-potential are derived from Eq. 2.22 as well, and can be calculated from the spatial derivatives of the real RF potential.

3.2 Trap geometry

3.2.1 Central and RF electrodes

The height of trap minimum purely depends on the geometry of the trap regardless of the RF frequency and the DC and RF voltages. To reduce the heating rate of this trap, we have decided to raise the height of trap minimum from 50 µm as is in [27] to 80 µm. This requires wider central and RF electrodes for the new trap. Since we want to make this 5-wire trap symmetric[1], so that it's easier to understand the behavior of the RF end-caps as will be discussed in the next section, the widths of the central three electrodes are decided to be 83 µm-100 µm-83 µm. This makes the trap minimum 81 µm above the trap surface.

As a prototype of the CMOS fabrication technology, this trap is only designed for $^{40}Ca^{+}$ ions. For proper quantum control, we require the axial trapping frequency to be at least 1 MHz. To align the ions in a chain and freeze out their radial motional degrees of freedom, we require the radial confinement to be about 2∼5 times the axial trapping frequency. Since the ion has been moved higher for this trap, we will need higher RF voltage or lower RF frequency to create the same radial confinement as before, according to Eq. 2.22. Thanks to the bigger mass of $^{40}Ca^{+}$ ions (comparing to Be^{+}), the q parameter for $^{40}Ca^{+}$ is still good for relatively low RF frequencies, according to Eq. 2.4, therefore we decided to lower the RF frequency to 40 MHz which relaxes the requirements for higher RF voltages. As a consequence, for the above mentioned RF and central electrodes geometry, a 70 V

[1] Normally an asymmetric geometry, where one RF electrode is wider than the other, is more favorable. One reason is that the trap axes will be tilted spontaneously, while for the symmetric trap, additional DC voltages have to applied to tilt the trap axes to allow the Doppler cooling with single laser beam. The other reason is that to create a certain confinement for the same height of the trap minimum, less voltages will be required for an asymmetric trap, since the ion is closer to the thinner RF electrode and therefore also closer to the DC electrodes on that side, which renders the voltages 'more efficiently' used to create the curvature.

RF voltage will provide $2\pi \times 2.97\,\mathrm{MHz}$ radial confinement at the pseudo-potential minimum, and a 100 V RF voltage provides $2\pi \times 4.25\,\mathrm{MHz}$ radial confinement.

3.2.2 Segmented DC electrodes

Segmenting the DC electrodes gives us more flexible control over the ions' positions and axial motions, allows the ion-transportation experiments, and makes it possible to define multiple traps on a single chip. Limited by the chip size[2], for this trap, the two DC wires are divided into 15 electrodes.

The width of each DC electrodes determines the amount of DC voltage needed to generate a certain axial confinement. To optimize this parameter, I have done a simulation to study the relation between the required DC voltage and the width of DC electrodes, where the central and RF electrodes are configured as discussed in the last section, only 3 pairs of DC electrodes are placed[3], and the necessary DC voltages to generate a 1 MHz axial confinement at the pseudo-potential minimum for different DC electrode widths are calculated. Fig. 3.1 shows the simulation result. According to this result, we decided to make each DC electrode 140 µm wide, so that the required DC voltage is close to the minimum while simultaneously we still have decent spatial resolution in controlling the ion's positions.

3.3 RF electrode end-cap

Ideally, we want the axial curvature of the RF potential to be constantly zero for all the trap minimum points along axial direction,

$$v_x(x, y_{\mathrm{trap}}, z_{\mathrm{trap}}) = 0, \forall x, \tag{3.1}$$

where y_{trap} and z_{trap} are the desired positions for trap minimum in $y - z$ plane. Therefore, according to Eq. 2.13, there would be no micromotion along the axial direction since $q_x = 0$, which will greatly benefit the ion transportation experiments along this direction. However, in reality this is hardly the case, since the RF electrodes are only of finite length, so at the ends of them there must be field lines bending axially, therefore contributing to the axial RF curvature. During the simulation, we have found that some

[2] In fact it is the wire-bonding pads for those electrodes rather than the electrodes themselves that take up space and limit the total number of electrodes. This will be discussed in the next chapter.

[3] 3 pairs of DC electrode is the minimal number to generate the axial confinement, and is also the optimal number. If 5 or more pairs must be involved to generate the wanted curvature, which will happen for thinner DC electrodes, then it's equivalent to 3 pairs of wider ones. Due to the limitation for the number of wirebonding pads, the former case is less favorable than just directly using 3 wider electrodes.

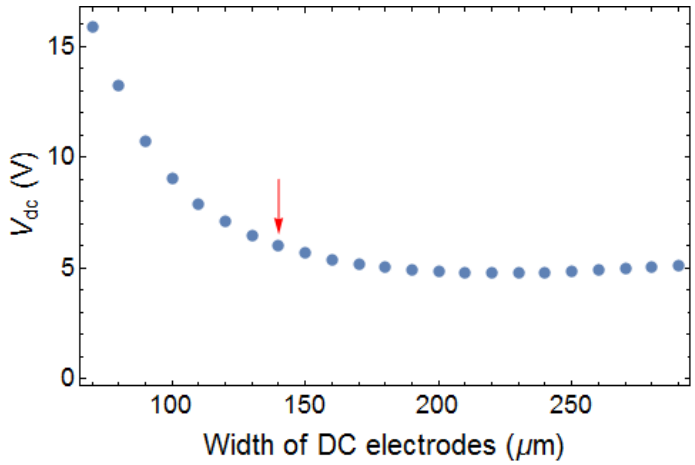


Figure 3.1: The span of DC voltages needed to generate 1 MHz axial confinement, for different widths of the DC electrodes. The width we have chosen (140 µm) is indicated with the red arrow. This is a trade-off between the required DC voltage and spatial resolution in the control over ions' positions and axial motions.

shaped end-caps added to the rectangular RF electrodes will decrease the axial curvatures of the RF potential at the trap minimum points[4]. Therefore I did more studies about such end-cap structures, and optimized their shapes to make the axial curvatures of the RF potential virtually zero at the trap minima.

For this purpose, first I have tried the 'OptimalFinitePattern' function in the SurfacePattern software package, where the optimal shape of the electrode fulfilling the given restrictions is returned. The result returned by 'OptimalFinitePattern' itself is not quite practical, since it requires applying intermediate voltages between 0 V and V_{RF} to parts of the RF electrodes. However, it does give us a hint that round shaped end-caps will help reducing the axial RF curvature. Therefore I modeled the end-caps by circle-segments with 3 free parameters, iterated these free parameters, and eventually found the practical optimal shape.

3.3.1 Optimization by SurfacePattern

The SurfacePattern package is not only able to solve the 'forward problem', where the shape of an electrode is given as input and the electrical potential created by it is returned, but also able to tackle the 'backward problem' with the OptimalFinitePattern function, where the optimal shape of the electrode is calculated on the given pixels, fulfilling the given restrictions. Realizing

[4]It is still not possible to eliminate the axial RF curvature for all points in the $y-z$ plane because the RF electrodes are still not infinitely long. In the following, all the axial curvatures of RF potential discussed are for the trap minimum positions in the $y-z$ plane, if not explicitly stated.

that some end-cap structures for RF electrodes can reduce the axial RF curvature, it is straightforward first trying to use this function to find the optimal shape of RF electrodes.

To use the OptimalFinitePattern function, first a pixel list must be defined, which indicates the places where the electrode under optimization can extend to. Therefore it provides the fundamental geometric restrictions for the electrode being optimized. Take our RF electrode to be optimized as an example, it must not overlap with the segmented DC electrodes, so the pixel list defined for it is as shown in Fig. 3.2. The middle part of the RF electrodes is limited by the presence of segmented DC electrodes, while at the two ends there is no more such restriction, so the RF electrodes is allowed to extend to at most $\pm 500\,\mu m$ in y-direction there, so long as the algorithm finds that will minimize the axial RF curvature. The middle part is defined as a $2100\,\mu m \times 300\,\mu m$ filled rectangle, where the size of the central DC electrode is not pre-defined. This allows the algorithm to find the optimal widths for the RF and the central DC electrodes.

Figure 3.2: The pixel list defined for the RF electrodes to be optimized, and sent to the OptimalFinitePattern function. The algorithm is allowed to extend the RF electrodes at their two ends, so long as the axial curvature can be minimized. However at the middle part, limited by the segmented DC electrodes, the RF electrodes are restricted to rectangular area. Note that the central DC electrode is not defined as *a priori* in this pixel list. This grants the algorithm the degree of freedom to optimize the widths of the RF electrodes and the central DC electrode.

The constrains for this optimization problem are given by the electrical potentials, the electrical fields, and the Hessian matrices of 25 sample points at the trap minimum positions evenly distributed along the axial direction. To make it easier for us to formulate the constraints, especially the constraints on Hessian matrices, and also for better understanding of the influence of the end-caps on the future experiments, we have adopted the symmetric geometry of the RF electrodes.

The electrical potentials at these sample points are set to 'Automatic', which means there are no actual constraints about them as they do not affect the dynamics.

The electrical fields for these sample points are restricted to

$$\vec{E} = (0, 0, 0).$$

According to Eq. 2.22 this restriction is defining those sample points as trap minima, which will be the central position of the trapped ions' oscillations.

Our desired Hessian matrix for these sample points is

$$H = \begin{pmatrix} 0 & 0 & 0 \\ 0 & \frac{\sqrt{2}m\Omega_{\mathrm{RF}}\omega}{QV_{\mathrm{RF}}} & 0 \\ 0 & 0 & -\frac{\sqrt{2}m\Omega_{\mathrm{RF}}\omega}{QV_{\mathrm{RF}}} \end{pmatrix},$$

where ω is the desired secular frequency, and V_{RF} is the RF voltage. The off-diagonal elements are set to 0, because the trap axes are not rotated, so the principal axes coincide with the Cartesian axes. H_{xx} is set 0 according to our requirement Eq. 3.1. H_{yy} and H_{zz} are calculated according to our desired secular frequency, based on Eq. 2.24. Here V_{RF} comes into the denominator as a normalization factor, because SurfacePattern only deals with unity voltage. The sign of H_{yy} and H_{zz} are opposite to fulfill the Laplace condition (Eq. 2.1).

The optimized electrode shape returned by OptimalFinitePattern is shown in Fig. 3.3. To generate a potential fulfilling the above mentioned constraints, the pixels in black color should be connected to the RF drive, while the white ones are to be grounded. The problem of this result is that there are grey

Figure 3.3: Optimized shape for RF electrodes returned by OptimalFinitePattern. The black pixels are to be connected to the RF drive, and the white pixels are to be grounded. The grey pixels are problematic, as intermediate voltages between 0 V and V_{RF} have to be applied to them, which are impractical.

pixels where intermediate voltages between 0 V and V_{RF} are supposed to be

applied. They are equivalent to small electrodes with various RF voltages. While in practice, building so many such small electrodes is too demanding and is therefore impractical. Supplying RF voltages to them is also challenging because practically it's hard to guarantee that the RF waveforms applied to them are in phase.

Although we can hardly realize such structure in practice, this result does give us a hint that RF electrodes with such round shaped end-caps will produce less axial RF curvature. Therefore, I described such end-caps with a circle-segment model with 3 parameters, and iterated the parameters to find the optimal practical shape which renders the least axial RF curvature.

3.3.2 Modeling with circle-segment

To find the optimal shape of the round end-caps, I modeled them as circle-segments with 3 parameters: the radius r, the height of triangular potion l, and the position of the center y (Fig. 3.4)[5], attached them to the normal rectangular RF electrodes, and solved the pseudo-potentials for them with the forward problem solver, ComputeFinitePotential. These three parameters are iterated and the ones producing the least axial peudo-potential are picked.

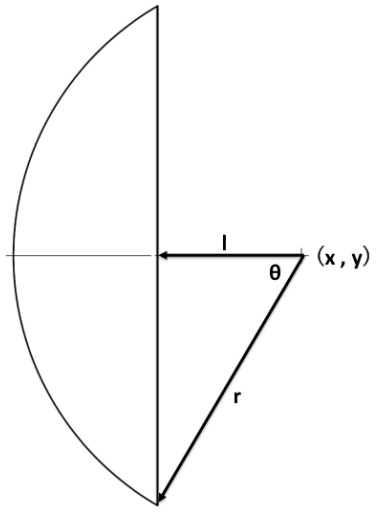


Figure 3.4: The circle-segment model for the round end-caps. Three parameters are used to describe it, namely the radius r, the height of triangular potion l, and the position of the center y. Since these end-caps are supposed to be attached to the rectangular part of the RF electrodes at the two ends, the x coordinate of the center is fixed by the length of the rectangular part, which therefore is no longer a free parameter.

[5]The x coordinate of the center is fixed by the length of the RF electrode, as the end-caps are supposed to be at the ends of RF electrodes. Therefore there is only 1 free parameter for the position of the center.

When using ComputeFinitePotential, I still treated the circle-segments as polygons, with n vertices. Tests have shown that when $n = 10$ the round curve is already well-approximated by a polygon. In the local frame centered at the circle center, the coordinates of the vertices are

$$x(i) = -r\cos(\frac{2i}{n-1}\theta - \theta),$$
$$y(i) = r\sin(\frac{2i}{n-1}\theta - \theta),$$

where $i = 0 \ldots n-1$, and θ is defined as $\theta = \arccos\frac{l}{r}$, which is shown in Fig. 3.4.

To speed up this optimization process, and also for better results, the numerical optimizer NMinimize provided in Mathematica, rather than simple nested loops, was used. The axial curvature of pseudo-potential, which is proportional to the curvature of RF potential according to Eq. 2.24 at the end of the trap[6], is used as the target function to be minimized with respect to the three free parameters r, l, and y.

The optimal parameters of the circle-segment shaped end-cap for the 83 µm-100 µm-83 µm RF-central-RF geometry are

$$r = 162\,\mu\text{m}, l = 43\,\mu\text{m}, \delta_y = 13\,\mu\text{m},$$

where δ_y is the offset for the end-cap in $y-$direction with respect to the inner edge of RF electrodes (see Fig. 3.6).

A comparison between the pseudo-potentials generated by RF electrodes with and without the optimized end-cap structures are shown in Fig. 3.5. The blue, solid lines are for the RF electrode with the end-cap structure, and the pink, dashed lines are for the RF electrode without the end-caps. Obviously the optimized axial pseudo-potential is flatter than the unoptimized one. The secular frequencies due to the pseudo-potential curvatures at the trap center and the loading zone ($x = 870\,\mu\text{m}$) for the optimized and unoptimized RF electrodes are summarized in Table 3.1.

3.4 Summary of trap parameters

To conclude this chapter, I will summarize the key parameters for this new trap in this section.

The geometry shown in Fig. 3.6 is realized with the top metal layer in the CMOS fabrication.

[6] In fact we want to minimize the axial RF curvature for every trap minimum point along the axial direction. By comparing different target functions, I found the axial curvature at trap end gives the best overall results for the curvatures at all the trap minimum points.

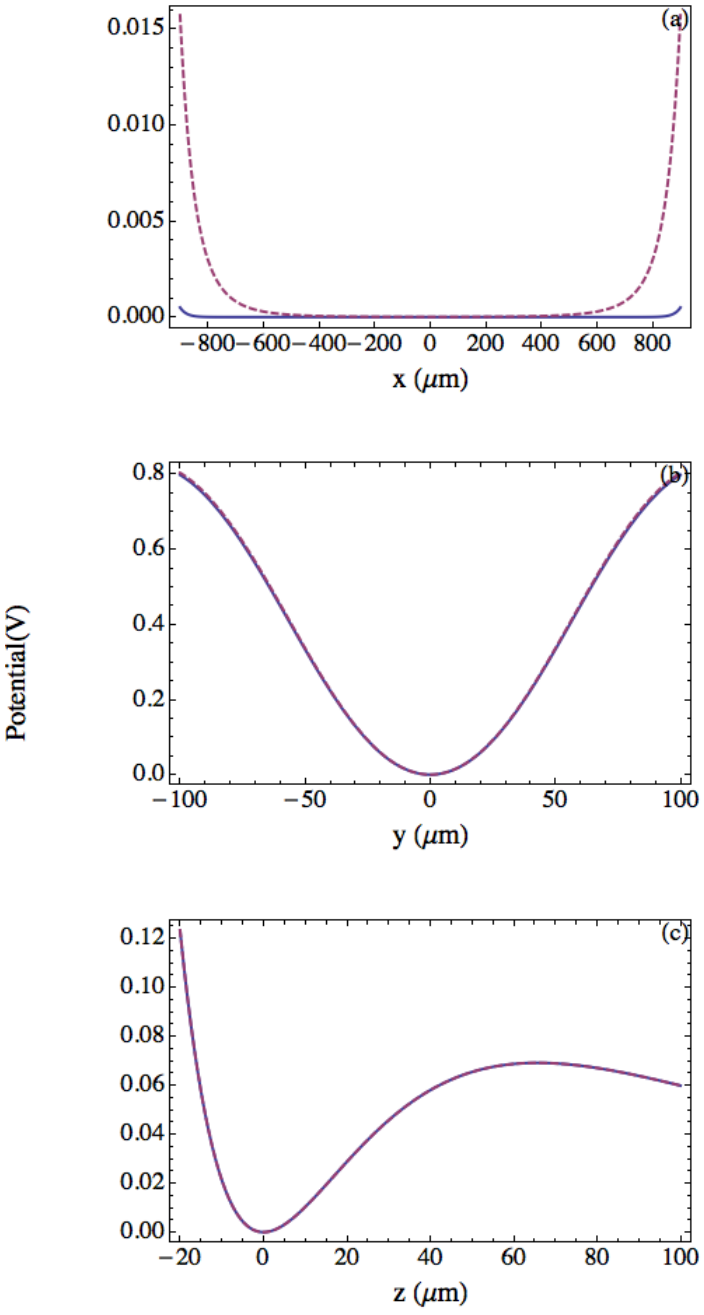


Figure 3.5: Comparison of the pseudo-potential with and without the end-caps. The blue, solid curve represents the pseudo-potential generated by the optimized RF electrodes, while the pink, dashed line is for the RF electrode without the end-cap structure. (a), (b), and (c) are the components along x-, y-, and z-direction respectively. A $100\,\mathrm{V}$, $40\,\mathrm{MHz}$ RF drive is used here for this calculation.

	Trap Center	Loading Zone
Optimized	(140 Hz, 4.25 MHz, 4.25 MHz)	(125 kHz, 4.37 MHz, 4.22 MHz)
Unoptimized	(4.08 kHz, 4.27 MHz, 4.23 MHz)	(441 kHz, 4.71 MHz, 3.51 MHz)

Table 3.1: Secular frequencies at the trap center and the loading zone, for optimized and unoptimized RF electrodes. The results are based on a 100 V, 40 MHz RF drive.

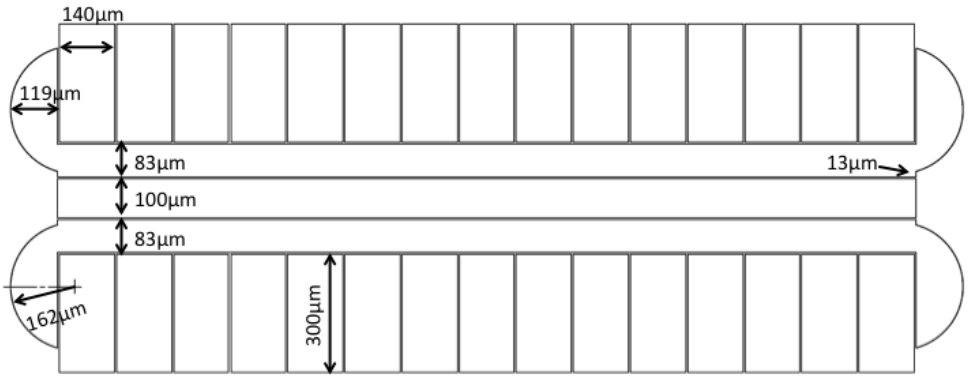


Figure 3.6: Geometry of the new SET trap. This structure is realized in the top metal layer of our CMOS chip. The only difference in the real layout from this figure is that 5 µm gaps are made between electrodes.

Fig. 3.7 shows the total potentials along x, y and z directions when both the necessary RF and DC voltages are applied to confine the ion in 3 dimensions. 40 MHz RF voltage with peak value 100 V is used here. The DC voltages are optimized for 1.5 MHz axial confinement, at trap center $x = 0$ for (a), (c), and (e), and at the desired loading zone $x = 870$ µm for (b), (d), and (f).

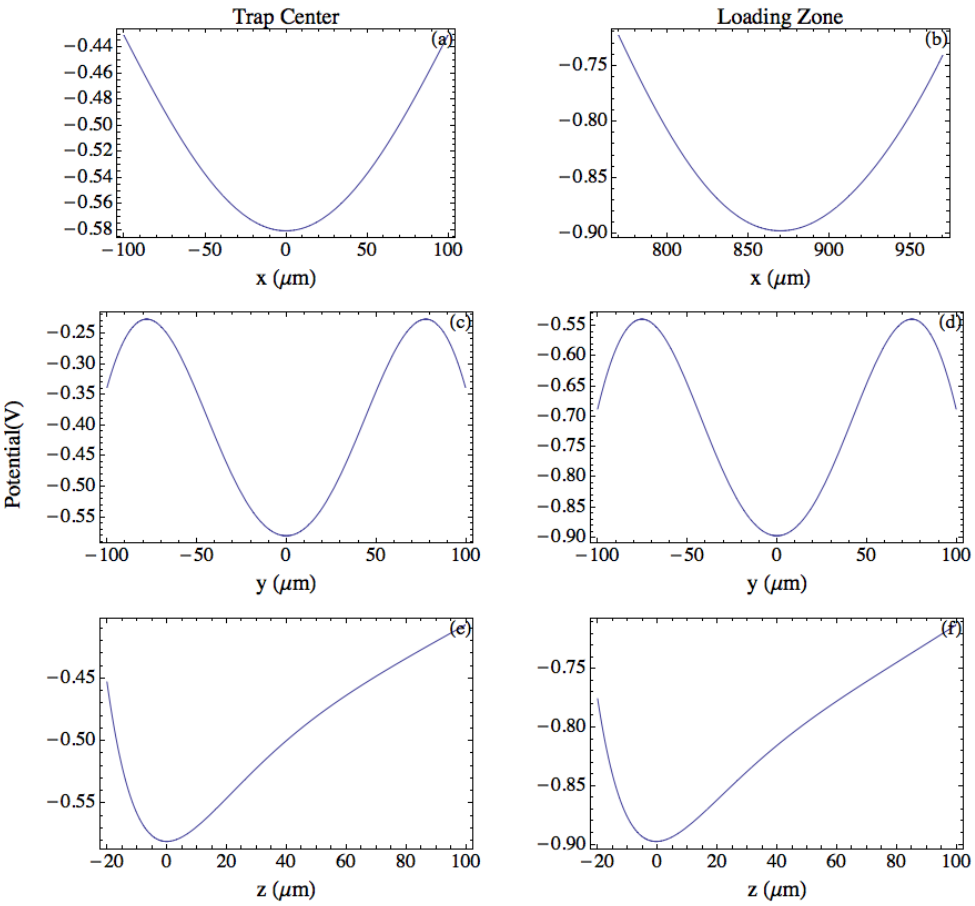


Figure 3.7: (a)(c)(e): the potentials along x,y,z directions when the DC field keeps the potential minimum is at the trap center. (b)(d)(f): the total potential in vicinity to trap minimum when the minimum is displaced to the loading zone, which centers at 870 µm. 40 MHz, 70 V RF is used here. The DC voltages are optimized for 1.5MHz axial confinement. Trapping frequencies along the 3 directions at the trap center are respectively 1.50 MHz, 3.75 MHz, 4.45 MHz. Trapping frequencies at the loading zone are 1.51 MHz, 3.95 MHz, 4.36 MHz.

Chapter 4

Chip design for CMOS foundry fabrication

Since the fabrication costs for microelectronic integrated circuits (ICs) are extremely high, it makes more sense for the small customers, like research groups, universities and small companies, who need only small amounts of chips, to join the multi-project wafer (MPW) runs held by the semiconductor manufacturers [28]. In the MPW runs, the designs from a number of customers are integrated onto the same wafer and then fabricated together at the foundries. The finished chips are diced and returned to each customer. In this way, the expensive costs for the masks, wafers, and fabrication processes are shared, making it affordable to manufacture the designs in small quantities. For us, joining such MPW runs makes the fabrication cost for each trap even less expensive than fabricating in clean rooms[1], and it's much easier to achieve the small features and the multi-layer structures from the foundry fabrication.

In different MPW runs [28], technologies with different linewidths (from 28 nm to 700 nm) and different numbers of metal layers (2∼7) are involved. Since at the current stage we only need structures at the length scale of tens of micrometers, and do not need very complicated structures involving many metal layers, the AMS 0.35 µm 4M technology H35B4D3 is selected, which is cost efficient and also best suits our time schedule.

In this chapter, I will first briefly overview the CMOS technology, and then discuss my design of the 4-layer structured CMOS chip. The practical considerations to ease our experiments and some necessary compromises to fulfill the design rules of the AMS 0.35 µm 4M technology will be included in the second part[2].

[1] 8553 Euro for 50 samples, with VAT included.

[2] According to the non-disclosure agreements signed with Europractice and AMS, as the

4.1 CMOS technology

Metal-oxide-semiconductor (MOS) transistors in n- and p- types (NMOS and PMOS) are the building blocks of the CMOS logic. By interconnecting them, single-bit and two-bit logic gates for classical computers can be realized, and this is how the word 'complementary' comes into the name. Comparing to the transistor-transistor logic (TTL), CMOS devices consumes much less power, because no standing current is needed when the state is not changing. Also, it benefits from short propagation delays, controlled rise and fall times, and better immunity to noises [29]. With decades of developments, CMOS now allows high density of logic gates. These reasons make it the most popular technology in the manufacturing of VLSI.

Historically, the gate of the MOS transistor was made of metal, and this was where the name 'MOS' came from. Since 1970s, heavily doped poly-crystalline silicon (poly-Si) has become the standard material for the gate, but the name 'MOS' remained to be used. Except for the most advanced transistors, where the metal gate is reintroduced and SiO_2 is replaced by some more advanced dielectric material, nowadays the gate material is still the heavily doped, highly conductive poly-Si [30]. The metal layers in the current CMOS technology are mainly used for inter-connecting the NMOS and PMOS transistors underneath to realize the logic gates. They are also used to form the wireboding pads which allow the connections of the chip to the outside world. It has recently been realized that these metal layers can also be utilized to form the electrodes of SETs [13]. This is a promising way to scale the SETs up, and moreover, thanks to the well-developed CMOS fabrication technologies, small structures, or complicated multi-layer structures are now open to the ion traps.

The cross section for a CMOS wafer and the deposited layers on top of it is shown in Fig. 4.1. The wafer is made of p-doped silicon. N-MOS transistors can be built by

- Heavily n-doping (n^+-doping) the desired regions to form the source and drain;
- Forming a thin SiO_2 insulator layer on top of the channel region between the source and drain;
- Building the gate with the poly-Si on top of the insulator.

To form a P-MOS transistor, first the desired region for the transistor has to be n-doped, and then the same procedures are applied. The only change

prerequisite to use the AMS technology, the details about the technology and the design rules contained in the confidential design manuals are not allowed to be revealed here. The technical descriptions about the technology in this chapter are based on open-sourced documents from the Internet, and the detailed values of the design rules mentioned in this chapter are intentionally omitted.

is that the source and drain regions are now p-doped. The N-MOS and P-MOS transistors can be interconnected to realize various circuit logics. The interconnections are made by the metal layers above them. Multiple metal layers are typically needed to realize the logics with high complexity. On top of the whole structure, there is usually a passivation layer formed with SiO_2 and Si_3N_4, which protects the top metal layer from physical scratching or chemical corrosion. But on top of the wireboding pads, this passivation layer must be removed. This extra process to remove the passivation layer on top of wireboding pads is called pad opening.

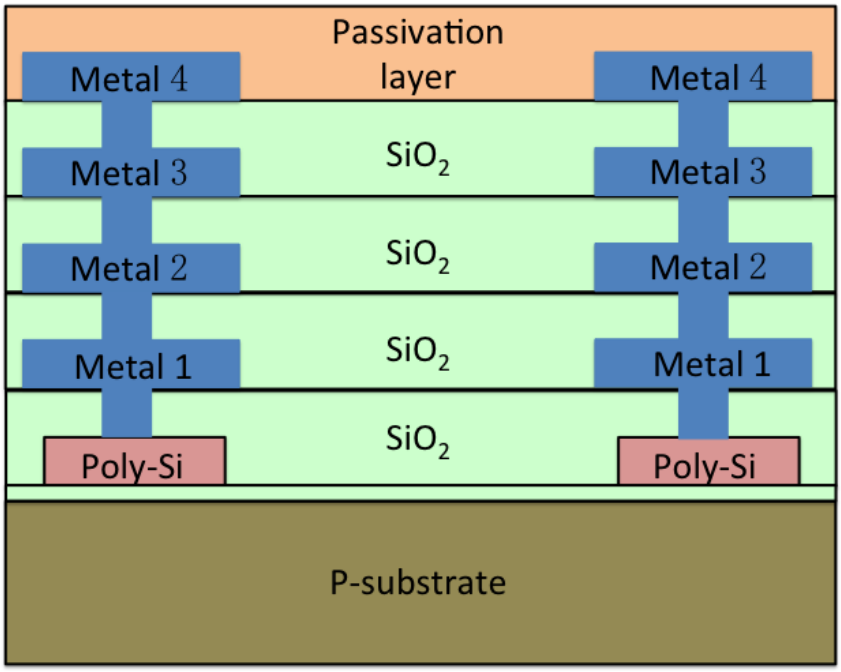


Figure 4.1: Sketch of the cross section for a CMOS wafer and the layers deposited on it. (Lengths not to scales.) PMOS and NMOS can be built on the substrate by doping (not shown), with the gate formed by the poly-Si layer. The metal layers connect each other and the N(P)MOS transistors with vias. Different layers are separated by SiO_2 layers.

As a prototype for the CMOS-fabricated SET, we decided not to integrate logic gates onto this chip, as making a circuit to work at 4 K environment is itself a highly non-trivial task. Therefore we are only utilizing the metal layers in Fig. 4.1. However, unlike the work in [13] where all tracks from the wirebonding pads to the electrodes are still routed on the top surface, I decided to make more use of the multi-layer structure, and route all the tracks in a separate layer. This grants us more flexibility in placing the

electrodes, saves space so that the chip can be made smaller, and makes the realization of the round end-caps of the RF electrodes possible, which otherwise have to be replaced by the tracks to the RF electrodes.

4.2 4-layer structure of the CMOS chip

According to [13], traps without a ground plane suffered from the laser-induced photo-effects due to the excitation of carriers in the silicon by the scattered 405 nm and 422 nm light. This effect changes the RF amplitude by varying the impedance of the trap, and is visible as ion motions synchronized with the 405 nm on/off state. A trap with ground plane will not suffer from this effect. For this reason, I have covered all the empty areas on the top metal layer (MET4), which are not occupied by any RF or DC electrodes, with ground plane. And I have also made the next layer underneath it, MET3, a ground plane. In case the laser-induced photo-effects excites the dielectric in the gaps between two electrodes, this MET3 ground plane can be helpful for the discharging, as the distance between two metal layers ($\sim$1 µm) is shorter than the gap between two electrodes (5 µm).

As is mentioned in literatures [8, 13], the p-doped silicon substrate can be RF lossy. Therefore a ground plane above the substrate is needed to prevent the RF electric fields from penetrating into the substrate. To prevent the RF leakage from the RF tracks into the substrate, I made the bottom metal layer (MET1) another ground plane, and do all the routing for the RF and DC electrodes in MET2, the metal plane between the two ground planes.

According to the design rules, at least a certain fraction of areas in each metal and poly-Si layer has to be filled by the corresponding material. Although we do not really need the poly-Si layer, dummy structures have to be placed there. Therefore I placed another ground plane in this layer covering the full plane.

Fig. 4.2 shows the scheme for the connecting and the grounding of our CMOS chip.

4.3 Layouts for each layer of the chip

The layouts of this chip are drawn in Cadence Virtuoso, provided by the Microelectronic Design Center of ETH. The design rule check is based on the AMS H35B4D3 technology. In this section, I will show these drawings for all the layers used by this chip, and discuss the technical requirements from the AMS design rule and the practical considerations to ease the future experiments.

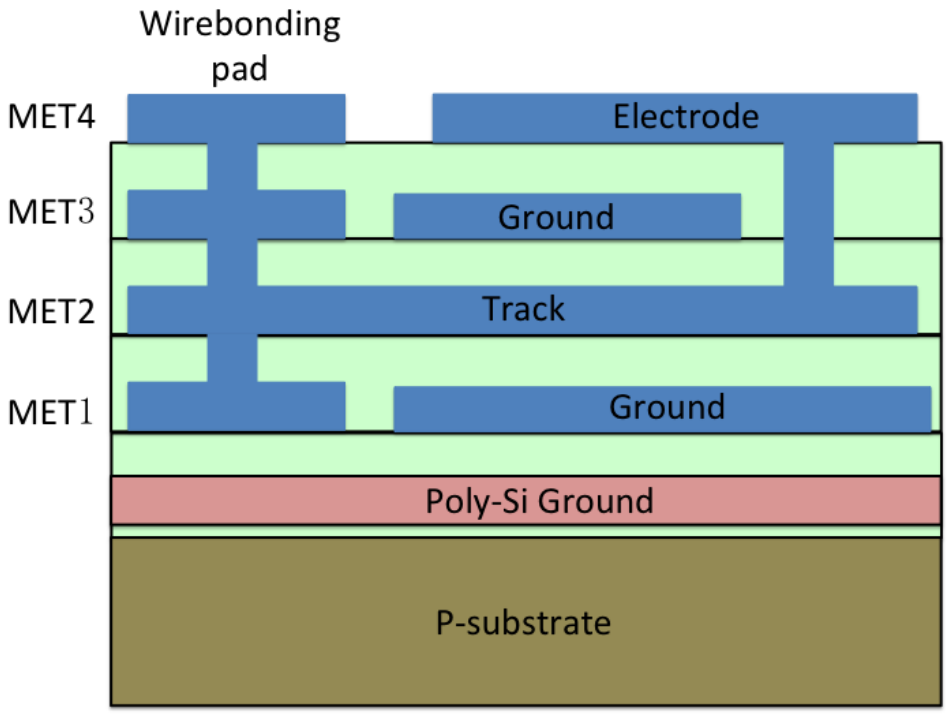


Figure 4.2: Sketch of the interconnecting and grounding scheme for the 4 layer structure. MET4 is used to build the electrodes for the trap. MET3 and MET1 are ground planes. MET2 is used to route the tracks from the wirebonding pads to the electrodes. Wirebonding pads are special structures which goes through all the metal layers. As requested by the design rule, at least a certain percentage of the areas have to be filled in the poly-Si layer. To fulfill this requirement, I made another ground plane in this layer.

4.3.1 MET4: top metal layer

The electrodes forming the SET and the wirebonding pads are placed on the top metal layer, MET4.

The trap lies in the center of this layer, and the shapes of its electrodes are as discussed in Chap. 3 and shown in Fig. 3.6, with the only difference being the 5 µm gaps between each two adjacent electrodes. Via arrays are placed on each electrode, connecting each electrode to its corresponding track routed two layers below. In the fabrication process, all the structures have to be described as polygons, whose vertices have to snap onto grids and only 45° and 90° corners are allowed. Limited by this, real circles are not actually possible. To build the round end-caps for the RF electrodes, I first draw a circle-segment with the parameters defined in Fig. 3.6, and then approach it with a polygon, whose vertices are snapped to 0.05 µm grids. Zig-zags can be seen in a zoomed drawing file. For our end-cap structures on the length scale of $\sim 100\,\mu m$, the effects of zig-zags on the length scale of

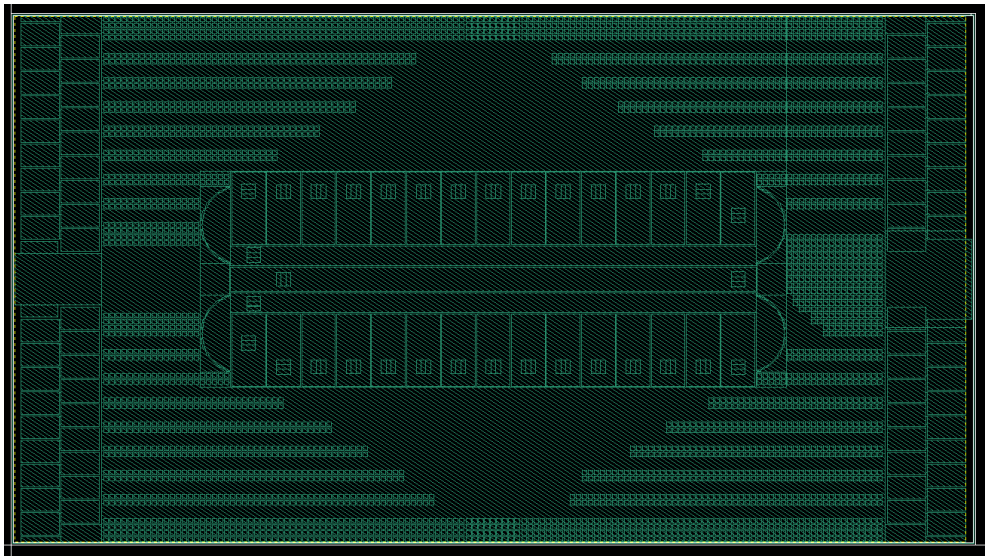


Figure 4.3: The layout for the MET4 layer. The electrodes for the trap are placed in the center. Wirebonding pads are patterned at the shorter edge of the trap. Two wirebonding pads are made for each electrode, with one being the backup. All the other areas are covered by a ground plane.

0.05 µm should be negligible, as they can hardly be seen by the ion.

The wirebonding pads are made 95 µm × 160 µm. For higher reliability, I have made two wirebonding pads for each electrode, one of which is used as backup. Therefore if the bonding pad for an electrode gets damaged, we will not have to discard the whole chip and do all the wirebodings again with a new chip. The numbers of wirebonding pads for the RF and the ground connections are further doubled, making the total count to 4. Two or four wires can be simultaneously bonded for the RF and the ground, which on the one hand provides higher reliability, and on the other hand reduces the resistances for these connections.

I have also made two pairs of wirebonding pads for the central electrode, routed to its two ends respectively. This opens the possibility to apply microwave to the central electrode. These two pairs of bonding pads are named 'CDC' and 'CMW', which are short for 'central DC' and 'central microwave' respectively.

To ease the wirebonding, I placed the name tag for each wirebonding pad next to that pad (not visible in Fig. 4.3 as they are too small). The name tag indicates to which electrode one wirebonding pad is routed, which is in the form of 'RF', 'GND', or 'UL3' (meaning the upper-left 3rd DC electrode). To minimize the size of the whole chip, which reduces the fabricating cost and allows tighter focusing of lasers[3], I tried to patten these bonding pads compactly. The eventual size of this chip is 2.2 mm × 4 mm, which is mainly

limited by the wirebonding pads.

For better laser accessibility, I put all the 36×2 bonding pads at the shorter edges of the chip, therefore nothing is blocking the laser on the longer edges, so the laser can focus onto any spot on the trap from a big range of angles. I have also left a 230 µm spacing between the wirebonding pads in the middle. This spacing allows the laser to shine onto the ion along the axial direction of the trap.

Except for the trap electrodes, the wirebonding pads and the necessary gaps, the whole surface is covered by one piece of metal which is connected to the ground. To shorten the ground loops, I have placed vias wherever possible which connect together the three ground planes in MET4, MET3 and MET1, and the grounded tracks in MET2[4]. These vias are visible as small squares in Fig. 4.3.

4.3.2 MET3: ground plane

MET3 layer is designed as a full ground plane as shown in Fig. 4.2. The layout for this layer is shown in Fig. 4.4.

According to the design rules, slots of certain size should be cut within wide metals for strain releasing[5]. An easier way to make the design is therefore replacing wide metals with bunches of periodically patterned thinner metal strips, so that this requirement is walked around. Using this strategy, I covered this layer with 22 µm wide metal strips separated by 3 µm from each other. I chose these two numbers to make the period of this pattern 25 µm, so integer numbers of such patterns can be used to fill the space whose width is integer times of 100 µm, which is indeed our case. To connect these separated metal strips together and also to shorten the ground loops, I placed vertical strips 22 µm in width and 278 µm in separation. These metal strips form a big ground mesh covering the whole plane. Arrays of vias are placed to connect this ground mesh to the ground plane in MET4, and the

[3]For a Gaussian beam, the smaller its beam waist is, the faster the beam size expands with the distance from its focus. To avoid the expanded beam being blocked by the trap surface, the beam waist is limited. For a smaller chip, the expanded beam is less likely to be blocked, so tighter focusing is allowed, which renders faster Rabi oscillation given the same laser power.

[4]Putting that many vias is actually an over-kill, but when doing the design I thought it would not do any harm at least. Later we heard from Lincoln lab that the vias could scatter light and should therefore be avoided on the paths of lasers. However by then the design was already submitted and could no longer be changed. Whether our chip will suffer from the same problem is still unknown. We need to evaluate the light scattering effect of the vias by experiments.

[5]Agreed by the manufacturer, this requirement is waived for MET4, since strain releasing slots on the trap electrodes will greatly affect the fields, and therefore invalid the whole trap design. But for the rest of the metal layers we had better stick to this design rule, which guarantees the best fabricating quality and lowers the risks of chip failure.

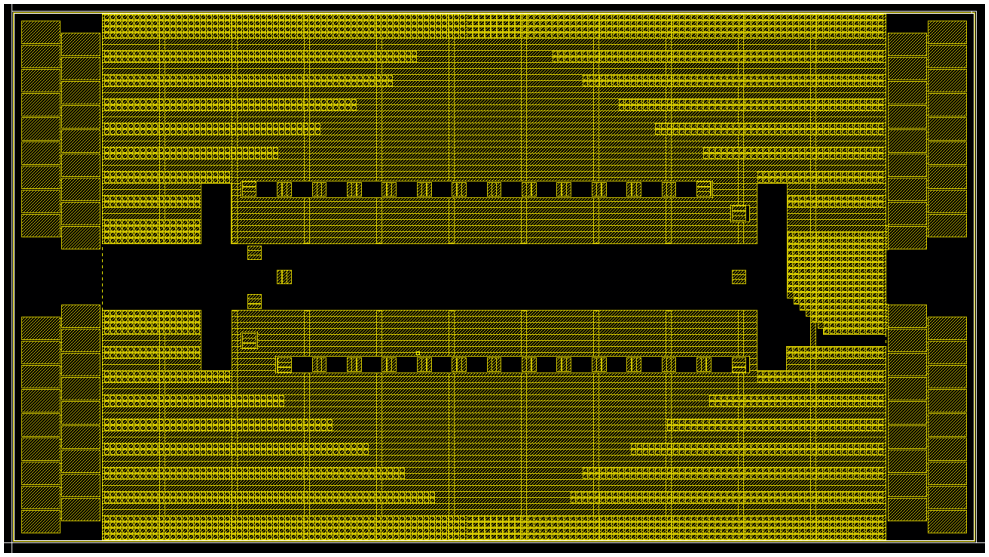


Figure 4.4: Layout for MET3 layer. 22 µm wide metal strips are patterned to avoid the mandatory strain releasing slots for wide metal. Vertical metal strips with 300 µm pitch are used to interconnect these horizontal ones. Cuttings are made to leave space for the vias connecting the tracks in MET2 and the electrodes in MET4. The parts of the ground mesh in parallel with RF electrodes and RF tracks are also cut to minimize the capacitance.

grounded tracks in MET2. Also this grounded mesh is directly connected to the wirebonding pads for the ground connection.

Since the vias have to go through this layer to connect the tracks routed in MET2 layer to the electrodes placed in MET4 layer, cuttings have been made on this ground mesh. In making these cuttings I made sure there is at least 5 µm clearance from each via array to its nearest grounded strips.

Calculations have shown that the parallel plate capacitor formed by the RF electrodes and the underlying ground plane contributes the most capacitance across the RF and the ground. This capacitance lowers the resonant frequency and the Q value of the RF resonator as characterized in Sec. 6.1.2. To minimize this capacitance, I have cut out the ground meshes right underneath the RF electrodes in MET4 and those right above the RF tracks in MET2. By doing this, the only ground plane in parallel with the RF electrodes is the one in MET1 layer, which has bigger separation from MET4, and therefore has less contributions to the capacitance.

4.3.3 MET2: routing layer

I have used the MET2 layer to route the tracks from the wirebonding pads to the spots right underneath their corresponding electrodes, and then use vias to connect these tracks to the electrodes. The layout for the MET2 layer is shown in Fig. 4.5. All the tracks are made 30 µm wide. Thinner tracks

will increase the resistance for the signals, while on wider tracks the strain releasing slots are obliged to be cut, which makes this layout unnecessarily over-complicated, and also cancels the benefit of the lower resistance we are gaining from the wider tracks.

The four RF bonding pads are connected together by a vertical metal strip in MET2, and two identical tracks lead the RF signals to the vias connected to the electrodes. The symmetry in the configuration of the RF connections avoids the phase difference in the RF fields on the two RF electrodes. These two RF tracks are made as short as possible, to reduce the resistance for the RF. In an older version, I have extended these two RF tracks to RF meshes, to further reduce the resistance for the RF. But calculations show that the resistance is actually mainly contributed by the bonding wires, since after all these RF tracks on the chip are much shorter comparing to the length of bonding wires. Extending the cross section of the RF tracks does very little help to the total resistance, while on the other hand the RF mesh will non-negligibly increase the capacitive coupling to the ground planes. For this reason, the RF mesh design is discarded and the simple RF tracks are kept.

Grounded tracks are placed into the spacings between each two neighbouring signal tracks, except for the two RF tracks. All the free area in this layer is also filled with the ground mesh same as MET3, and the same cuttings in the central part are made to reduce the capacitive coupling between the RF electrodes and the ground. Via arrays are placed on the grounded tracks, which connect these tracks to the ground planes in the upper and lower layers.

4.3.4 MET1: ground plane

The bottom metal layer, MET1 is also used to form a ground plane. To avoid wide metals, I used the same strategy here as in MET3, by filling this layer with 22 µm metal strips separated by 3 µm. The same 22 µm vertical strips with 300 µm pitches are used to interconnect them. Unlike the MET3 layer, there is no need to cut the openings for the vias. And since this ground layer is meant for preventing the RF from penetrating into the RF lossy substrate, the cuttings underneath the RF electrodes are left out as well. But since this ground mesh is too close to the RF tracks in MET2 layer, I kept the cutting of the ground mesh under the tracks.

4.3.5 Pad opening

As is discussed in Sec. 4.1 and shown in Fig. 4.1, there is a passivation layer made of SiO_2 and Si_3N_4 above the top metal layer, providing protections to the metals. The only exception is the wirebonding pad, where such passi-

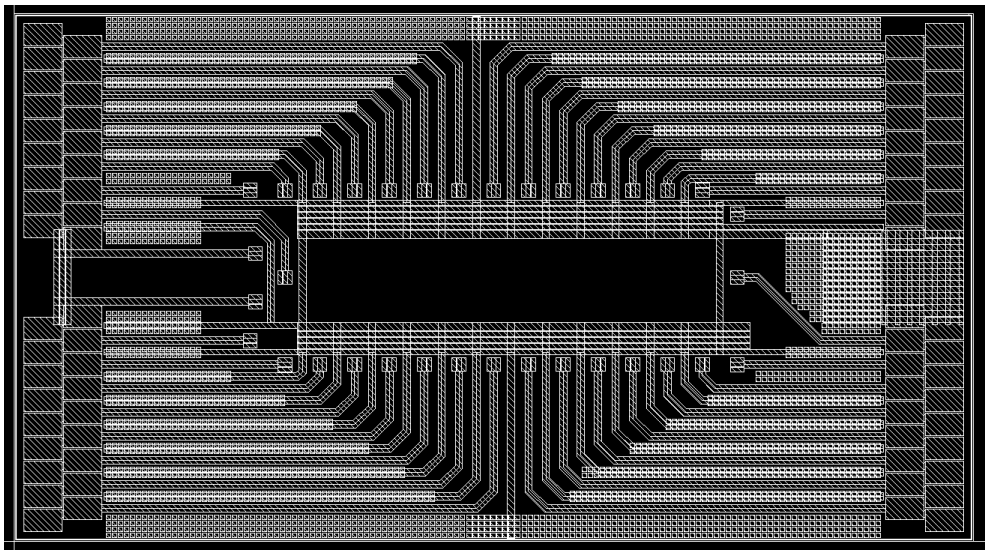


Figure 4.5: Layout for the MET2 layer, which is used for routing the tracks. $30\,\mu m$ wide tracks are used. The RF bonding pads are connected at the very first place, and two identical RF tracks lead the signal into the RF electrodes. The RF tracks are made as short as possible. In between other signal tracks I inserted grounded tracks, with vias connected to the upper and lower ground planes. The same ground mesh and the cuttings as MET3 are made in the central region of this layer to fill up the free space.

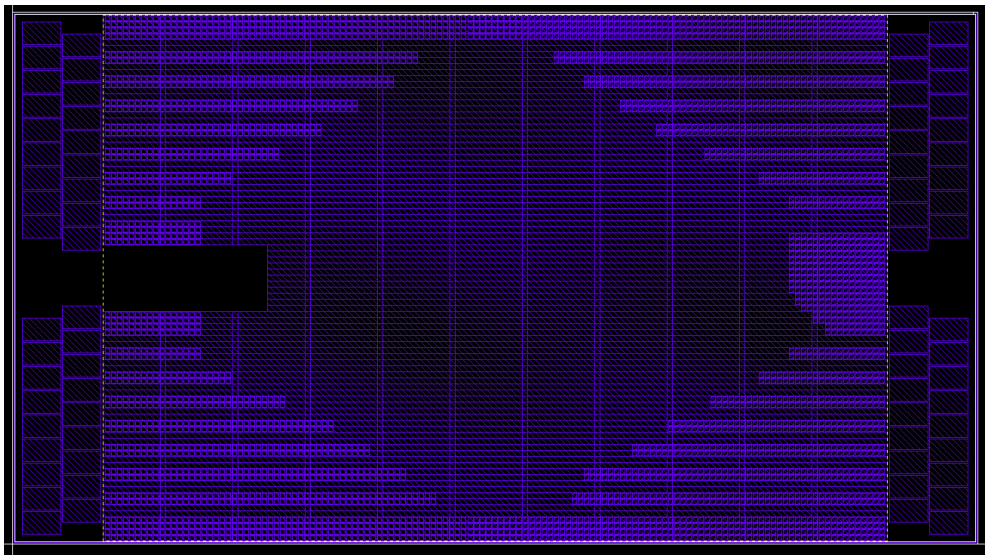


Figure 4.6: Layout for the ground plane in MET1 layer. Same as the ground plane in MET3 layer, I used $22\,\mu m$ wide metal strips with $3\,\mu m$ separation to fill up this layer. The only difference is that no cuttings are made in this layer, since there are no vias to go through this layer, and the RF fields are to be shielded by this plane from penetrating into the RF lossy substrate.

vation layer has to be removed to expose the metal which allows electrical connections to the chip. In Cadence Virtuoso, the regions where the passivation layer is to be removed are drawn in a 'PAD' layer. This layer gets its name because normally the removal of the passivation only happens for the wirebonding pads.

Since in our case we need the electrodes to be exposed, and this passivation layer will anyway suffer from the laser-induced photo-effects as discussed in [13], we want the passivation layer to be removed from the whole chip. To achieve this, in addition to all the wirebonding pads, I have covered all the trap electrodes and the whole ground plane, as well as the regions where the laser might pass, with the PAD layer, as is shown in grey in Fig. 4.7.

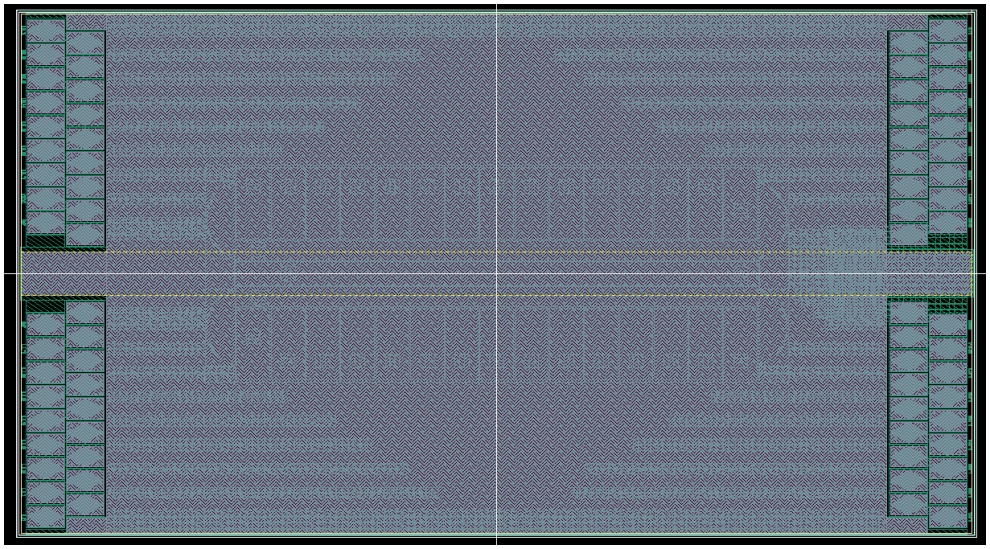


Figure 4.7: The PAD opening layer which indicates the regions where the removal of passivation layer will happen (grey color). As a reference, the MET4 layer is also shown here. The tags for each wirebonding pad as discussed in Sec. 4.3.1 can be seen in this figure.

Chapter 5

Backside-loading slot

The accumulation of metallic atoms on the surface of the trap may cause short connections of the electrodes. This is a common failure mode for SETs [8]. Moreover, it has been observed in previous experiments that the contamination of the trap surface by the neutral atoms will also increase the motional heating rate of the trap. In our current loading scheme, the neutral atomic flux emitted from the atomic oven is aligned in parallel to the trap. Then the atomic flux will inevitably have velocity components towards the trap surface, which cause the atoms to accumulate on the surface. One solution to this problem is to mill a loading slot through the trap, so that the oven can be placed behind the trap. The neutral atoms emitted from the oven will then fly through this loading slot, and get trapped above the trap surface. In this way, the atoms emitted from the oven will only have velocity components leaving the trap surface, so the contamination of trap surface is minimized.

Since we are sharing the silicon wafer with other customers of AMS, so the industrial standard technology has to be used (where materials are deposited layer by layer to form the CMOS structures), it is impossible to have this loading slot directly made during the chip fabrication process. Therefore we have to find proper ways to mill this slot ourselves. For this task, I did some research about the possible milling or etching technologies, and contacted the relevant cleanrooms equipped with the corresponding facilities. In the end, focused ion beam (FIB) was chosen due to its material compatibility and decent milling speed.

In this chapter, I will first overview and compare the milling and etching technologies I studied, and then discuss the specific FIB milling strategy for our chip, and my preparations for it.

5.1 Reactive Ion Etching

Reactive ion etching (RIE) is one kind of plasma-assisted dry etching, which is able to produce very anisotropic etch profiles. Its basic idea is quite simple [31]: two parallel plates (similar to a parallel plate capacitor) are placed in a plasma chamber, and high power[1]of RF field (typically 13.56 MHz) is applied to them. Gas of certain molecules, whose species depend on the material to be etched, is injected into the plasma chamber, gets ionized under the strong oscillating field, and forms plasma. The ionized molecule is able to chemically react with the material to be etched, and this is where the name 'reactive ion' comes from. The electrons striped from the gas molecules and the left positively charged reactive ions will move up and down driven by the RF field. Due to the bigger mass, the ions will respond less to this oscillating field than the electrons. The sample to be etched is placed between the parallel plates, but electrically isolated from them. Therefore, when the electrons are absorbed by the sample, negative DC biasing is build up there. This negative DC biasing forces the positively charged massive ions to drift towards the sample, and chemically react with the sample materials not protected by the mask. The reaction product is thereafter pumped out so that it won't block the further chemical reactions between the ions and the sample material. Since the reactive ions are mostly driven to the sample vertically by the electrical field, RIE can produce much more anisotropic profiles than wet etching.

Two RIE facilities are available in FIRST lab at ETH Zürich, namely the RIE 80, which etches dielectric layers and photoresists, and RIE 76, which etches metals, polymers and other materials. However, the main problem of them is the forbiddingly slow etching rate. According to the manual for RIE 80, provided by FIRST lab, the typical etching rate for SiO_2 is about 58 nm/min for rapid etching mode, and about 24.5 nm/min for normal etching mode. By consulting the operator of RIE 76[2], I leaned that the etching rate of RIE 76 for silicon and SiO_2 is compatible to RIE 80, while the 'etching' of metal is more like sputtering with Argon, whose 'etching rate' is only about 5 nm/min. To etch through our chip, which has a roughly 10 µm functional layer, which consists of metal and SiO_2 layers, and a silicon substrate about 250 µm thick, RIE would take much too long.

[1] 500 W for RIE 80, which etches dielectric layers and photoresists, and 300 W for RIE 76, which etches metals, polymers, and other materials. These are the two RIE facilities available in FIRST lab.

[2] Emilio Gini, gini@first.ethz.ch

5.2 Deep Reactive Ion Etching

The low etching rate makes RIE only suitable for etching small structures. An advanced version of it is the deep reactive ion etching (DRIE), which is faster in etching rate and therefore is able to make deeper features. This technology is used in [11], to excavate trenches on the silicon wafer.

Maintaining the high anisotropy when excavating deeper structures is the main challenge for DRIE, because unlike the top surface, the sidewalls of the trenches are not protected by masks, therefore can be horizontally etched by the chemical reactions with the reactive ions. To keep the high anisotropy during the deep penetration, nowadays there are two main process technologies utilized in DRIE [32]: cryo-etching and Bosch process.

In the cryo-etching process, the substrate is cooled (usually to about $-120\,^{\circ}\mathrm{C}$), and the normal RIE as discussed before or the inductively coupled plasma (ICP) RIE with denser plasma is used for the etching. The cooling down of substrate slows down the chemical reaction on the unmasked sidewall surfaces, but does not stop the reactions on the target area vertically exposed to the ions due to the higher concentration of reactive ions there, therefore leads to anisotropic etching behavior.

For samples which cannot withstand the low temperature in the cryo-etching, the Bosch process is the choice, where the etching process with the reactive gas and a deposition process with the protective gas are alternated periodically. In the deposition phase, the protective gas forms a polymer layer on the surfaces including the sidewalls. And in the etching phase, the protective polymer layer vertically exposed to the reactive ions is quickly removed by the bombards with the ions, and the etching of substrate continues, while the protective layer on the sidewalls is hardly affected. Therefore an isotropic feature is created. The duration of each etching/depositing cycle is several seconds or 10-20 seconds. The shorter the cycle, the higher anisotropy can be achieved, but the overall etching rate is lowered.

Comparing Bosch process, cryo-etching consumes longer time, mainly because the sample needs to be cooled to cryo-temperature, and have to warm up to room temperature after the etching finishes. But cryo-etching provides smoother sidewalls due to its continuous nature. The Bosch process usually have ripples, because the deposition and etching processes are alternated.

To explore the possibility to etch our desired loading slot with DRIE, I contacted 3 cleanrooms with such facility: the FIRST-CLA clean room run by the Institute for Mechanical Systems in ETH, the clean room of Department of Biosystems Science and Engineering (D-BSSE) in ETH, and the Binnig and Rohrer Nanotechnology Center (BRNC), a clean room in IBM Zurich lab. The answer from them is that there is no problem etching our 250 µm substrate with DRIE, and it can be quite fast (about 2 hours for the cryo-

etching in D-BSSE clean room). However etching the 10 µm functional layer is problematic, as those materials do not chemically react with the reactive ions for etching the silicon (in FIRST-CLA cleanroom, metal is not even allowed for the DRIE facility). To etch the mixed structure, like our CMOS functional layers, either several (D)RIE processes with different gases have to be combined, as is proposed by BRNC, or physical milling methods like the ion beam etching (IBE) are to be used, as proposed by FIRST-CLA and D-BSSE cleanrooms. The estimate time for etching our 10 µm functional layer with IBE is about 6 hours, according to the D-BSSE cleanroom.

The necessity of combining several technologies makes the DRIE approach too complicated. The time consumption to finish one loading slot (which should be around at least 10 hours including the sample preparation time for each etching stage) is not advantageous comparing to the plasma FIB as will be discussed in the following section at all. For these reasons, we decided the DRIE is not the correct way to go, and determined to mill the loading slot with FIB.

5.3 Focused Ion Beam

Unlike the chemical etching methods discussed above, FIB is a physical material removal method, where the ion beam scans at the region to be milled, and the ions with high kinetic energy sputters the material away from the sample. As a physical milling method, FIB does not have as strong material selectivity as the (D)RIE. This makes it the better choice for us to mill our CMOS chip with mixed layer structure.

FIBs are provided to ETH users by the Scientific Center for Optical and Electron Microscopy (ScopeM). For this task, we are using the Xe plasma FIB, Tescan Fera 3, which was installed only in December of 2014. This plasma FIB provides much faster milling rate than the conventional Ga-FIBs, which saves us the necessity to mechanically thinning the chip first. To start the FIB, the user just needs to locate the FIB beam to the region of interest, draw the shape to be milled, set the milling depth and choose the ion source current. A scanning electron microscope (SEM) is equipped in this machine, which is used to locate the FIB beam, and to monitor the FIB milling process in real time.

5.3.1 Practical issues

There are two practical issues when operating the FIB, which affect our milling strategy, and therefore determine the preparation work we have to do for this process, like the design of the proper sample holder. One is the trade-off between the milling rate and the milling accuracy, and the other is the difficulty in locating the ion beam when milling from the backside.

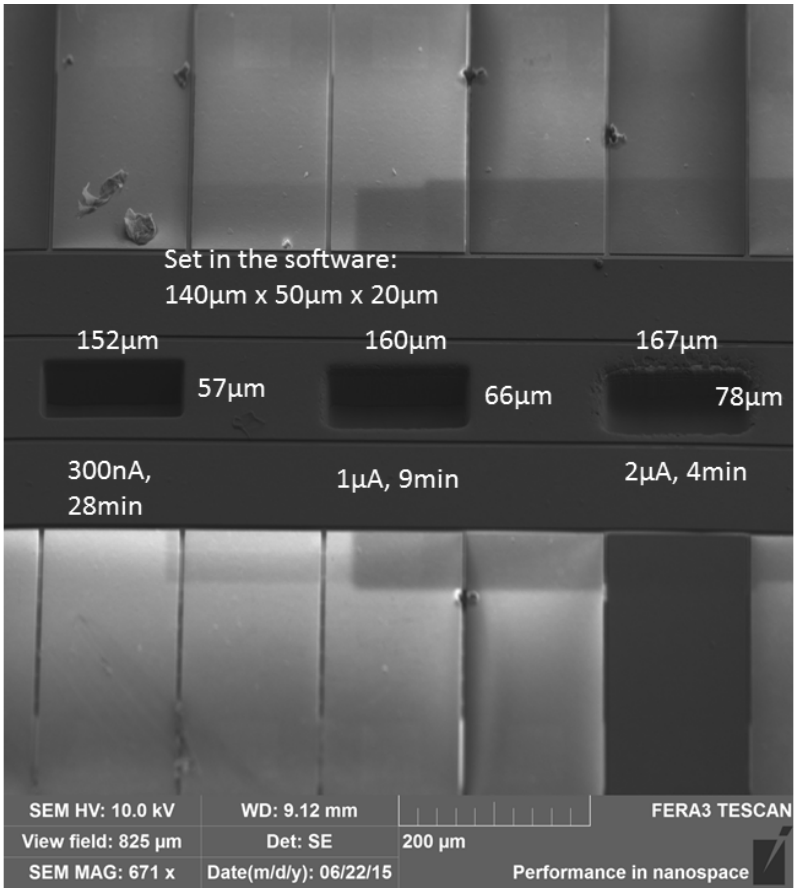
Essentially the only parameter affecting the FIB milling performance is the current for the ion source. The higher this current, the more ions are emitted from the source in unity time, and therefore the faster the milling process will be. However, although the ion beam is well-focused, the beam tail in the spatial beam profile will also sputter some of the material on the sample away, creating over-milling. The over-milling effect gets manifested when the beam gets stronger, i.e. high source current is used.

To evaluate the effect of the over-milling and find the optimal source current for our project, I did a comparison of the milling results for several settings for the current, as is shown in Fig. 5.1. In this test, I used 300 nA, 1 µA and 2 µA currents to mill a 140 µm long, 50 µm wide, 20 µm deep trench. The actual sizes of the trenches are all bigger than the desired value, due to the over-milling by the beam tails. The higher the source current, the bigger the actual size is. From the image taken by light microscope we can see, for 2 µA current, the over-milling has almost cut the central electrode into two pieces, which will result the failure of the trap. 1 µA works fine but poses stricter requirements for positioning the beam, otherwise the neighbouring RF electrodes might also be milled. For the safety of our trap, 300 nA seems the highest current we can use.

Since the milling from the frontside of the trap is limited to relatively low source currents, and milling through the whole chip with such low currents will be very time consuming, the natural choice for us is to first mill from the backside with the highest current for a certain depth, and then mill from the frontside with lower currents to finish the slot. Then we meet another practical challenge: positioning the ion beam on the backside of the chip.

Positioning the ion beam on frontside is straightforward, because we can see all the electrodes under the SEM, and use them as a reference. But if we flip the chip and start working on the backside, there is no such positioning reference any more. A way of positioning the ion beam to our region of interest is to measure the distances with respect to the chip edges. However, the precision of this method is poor due to the following reasons:

- The distortion in the imaging system. The distance measurement has to be done under the SEM. For lengths in smaller scales, the measurement is relatively accurate, but in the order of mm, the distortion effect of the system becomes non-negligible. This might be the leading source of imprecision in the positioning of the beam.
- The uncertainty in the size of the chip. The chips are not manufactured piece by piece. Instead, they are fabricated on a wafer, and then diced into pieces. Although our chip is designed to be 2.2 mm $\times$ 4 mm, the dicing does not necessarily happen at the center line between two chips, and therefore renders the uncertainty in the length and width



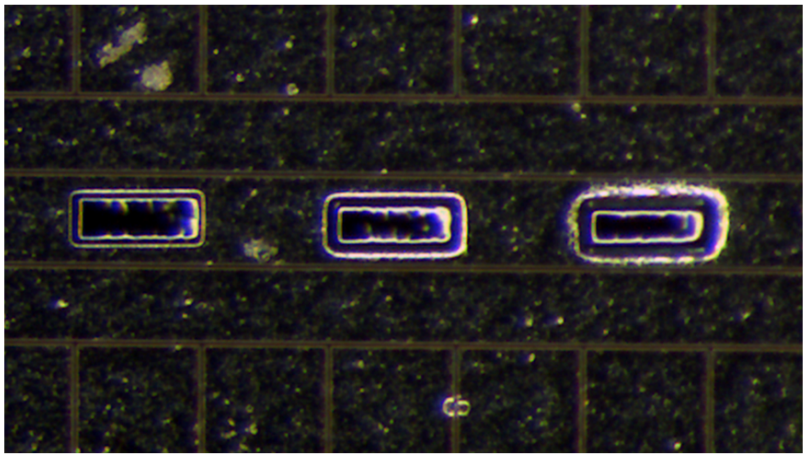


Figure 5.1: Comparison of the over-milling effects for 3 source current settings. Above: the image taken by SEM. Bottom: the image taken under light microscope. A $140\,\mu m$ long, $50\,\mu m$ wide, $20\,\mu m$ deep trench is set to be milled in the control software. $300\,nA$, $1\,\mu A$ and $2\,\mu A$ are used. As can be seen, due to the over-milling, the actual sizes of the trenches are all bigger than the desired value, and the over-milling gets worse when higher current is used. From the light microscope image at the bottom we can see, the central electrode is almost cut into two pieces by the over-milling of $2\,\mu A$. This might cause the failure of the trap.

of each chip. If we position the ion beam based on the designed size, offsets may exist.

- Limitation of the FIB's view field. Unlike the SEM, whose magnification can be adjusted in a wide range, the view field of the FIB is fixed, which is 410 µm × 410 µm. This means when drawing the milling region for the FIB, the edges of the chip are far out of the view field, so the position of the milling region cannot be directly measured from them. Intermediate reference points, like dusts on the back of the chip, or artificial markers milled by the FIB (Fig. 5.2), has to be used to. Errors inevitably accumulate in these 2-step or 3-step indirect measurements.

Due to these reasons, positioning the milling region on the backside of the chip becomes the most challenging part when operating the FIB.

5.3.2 Milling strategy

Since milling from the front side with a mild current will be too slow, while positioning the beam on the backside of the chip is rather imprecise, we came up with a 3-step milling strategy:

1. Mill a hole through the sealing ring of the chip, from the front side of the chip. Then determine the coordinates of our desired loading slot with respect to this guiding hole. This hole translates the spatial information from the front side to the back side. In this way, the uncertainty in the chip size will no longer play a role, and since the distance measurements are done with the same apparatus for both sides of the chip, the influence of the image distortion will be maximally cancelled.
2. Flip the chip, and mill a bigger opening (for example, twice as long and as wide as our desired loading slot) at the desired position, determined with respect to the guiding hole. This opening can be milled with the highest source current 2 µA to reduce the time cost, and its depth can be set to about 240 µm. The positioning of this opening will still need 2-step or 3-step measurements, but thanks to its big size, we will have bigger tolerance for the positioning imprecision, as long as this big opening contains the actual loading slot we want.
3. Flip the chip again, and finish the last 20 µm of the opening with a mild current (300 nA or smaller). With the electrodes as reference, the positioning of this opening can be very precise.

Milling the big opening from backside will take about 3.5 hours, and the shallow and small opening from front side will take about 0.5 hour. Including the time necessary for starting the system, mounting the sample, flipping the chip and remounting it, and positioning the beam on backside

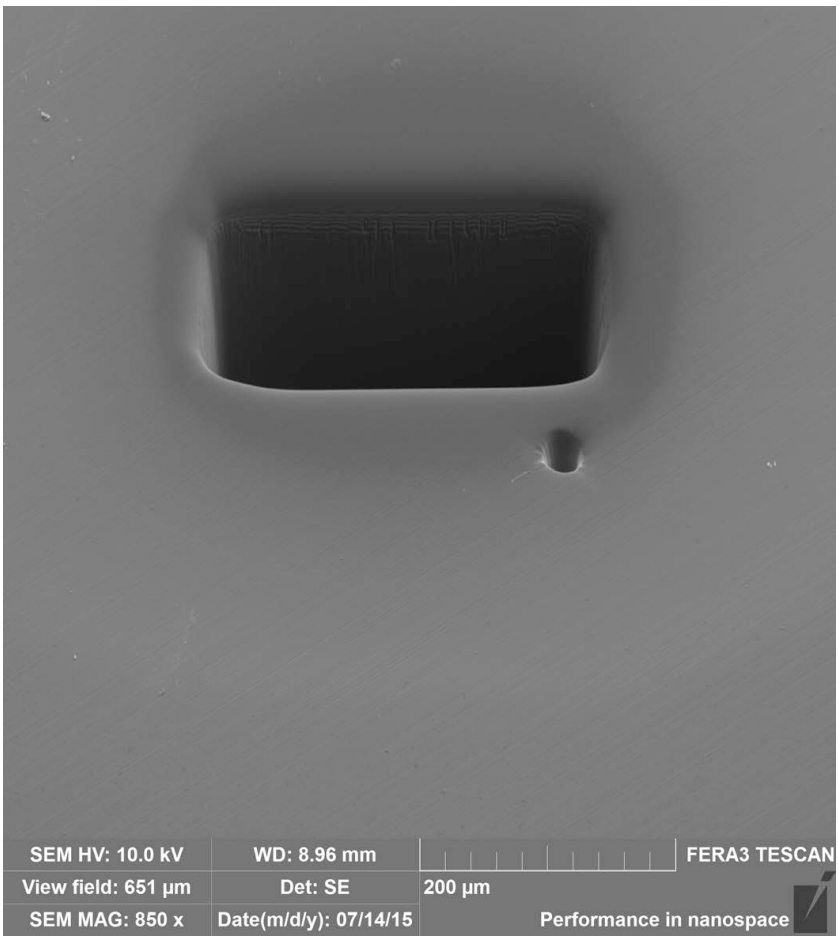


Figure 5.2: The reference marker milled by FIB, and the opening on the backside of the chip. First the coordinate of a dust particle (not shown) was measured with respect to the edges of the chip, and then this point marker is milled with respect to that dust. Finally the region to be milled is determined with respect to this marker. The accumulation of error in this 3-step measuring process make the positioning accuracy of the milling region rather poor.

(which takes the longest time), the estimated total time cost for milling one loading slot would be 6-7 hours. However the 3.5 hour waiting time for the big opening is essentially free time, and other small tasks can be scheduled then.

5.3.3 Chip holder for the FIB process

If we only need to mill the loading slot from the front side of the chip, we can simply glue the backside of the chip onto the chip carrier for the FIB machine. But since we need to put the chip face-down and mill from the back, this simple solution doesn't work, as the epoxy will contaminate the trap surface and can be hard to remove. Therefore we have to design a proper chip holder for this task, which provides mechanically stable supports for the trap, and avoids scratching of the chip surface as much as possible.

As the SEM has to be used to position the ion beam, the chip holder must be made of metal, otherwise the charges coming from the scanning electron beam will accumulate on the insulator surface, and greatly affect the SEM imaging. For this reason I decided to build this chip holder out of copper, which is softer than the Al trap surface. Therefore if scratching indeed happens, it's more likely that the chip scratches the chip holder, rather than vice versa.

On the top surface of the chip, the trap electrodes and the wirebonding pads are the key structures which we have to protect from scratching by all means. So the idea of the chip holder is to support and clamp the chip on those less critical areas. For this reason, I made the 2 mm long, 0.4 mm deep V-groove on the chip holder (Fig. 5.3). When the chip is fixed by two such chip holders, the long edges of the chip are clamped into the V-grooves. The 0.4 mm depth guarantees the trap electrodes in the center of the chip will by no means be touched by the holders. The 2 mm length of V-groove is only half the length of the chip, so as long as the middle point of the chip long axis is roughly aligned with the middle point of the V-groove, the wireboding pads on the two shorter edges are also safe from scratching. The benefit of the V-groove shape is that only the edges of the chip are touched by the chip holder. This feature further reduces the risks that the chip is scratched.

Two such chip holders are to be fixed into the sample carrier provided by ScopeM which fits the FIB facility. One holder can be glued onto the sample carrier, and the other one is flexible, which can be fastened by screw to clamp the chip. One practical problem is that the flexible chip holder always tends to tilt when being screwed. To solve this problem, I have made two features on the chip holders. Four guiding holes are drilled at the two ends of the chip holder. Stiff copper wires can thread through these holes on the flexible holder, and then those on the glued one. These wires will limit the tilting and up-down movement of the flexible holder, and only allow it to

be pushed forward by the screw. Besides, the lower half of the chip holder is extruded. Tilting to some extent will be limited by the extrusions as well, because a little tilting of the holder will renders the two extrusions touch each other and therefore the tilting is stopped by them.

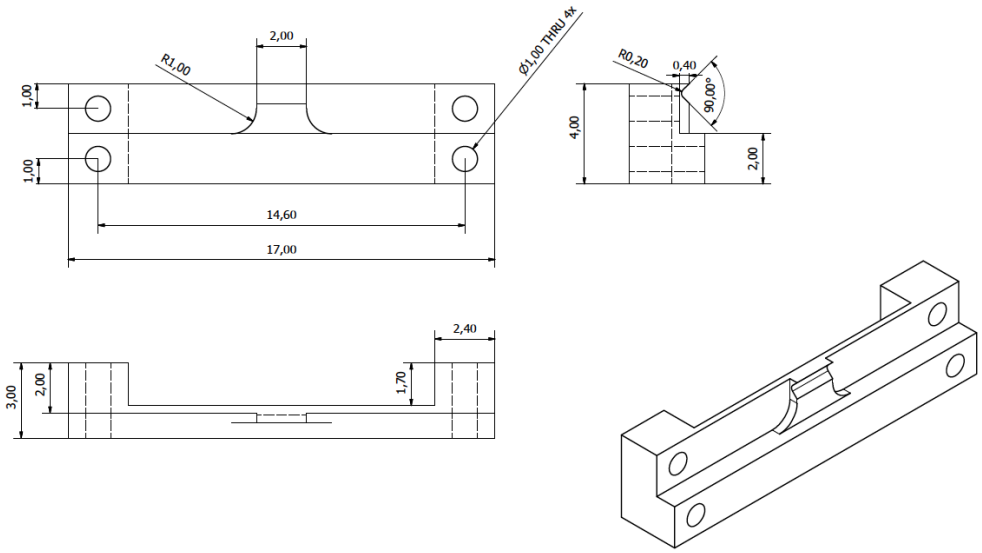


Figure 5.3: The drawing of the sample holder for the FIB milling process (1 piece). All units are mm. The material is copper. Two such holders will fit into the sample carrier provided by ScopeM. One can be glued onto the carrier, and the other flexible one can be fastened by the little screw on the carrier. The long edges of the chip will be clamped in the 2 mm long, 0.4 mm deep V-grooves of the two holders. The size of this V-groove is designed to guarantee that the trap electrodes and the wirebonding pads will not be touched when the chip is clamped by the holders. Copper wires are to be thread through the 4 holes at the two ends of the holder, to prevent the flexible holder from tilting when the screw is fastened. The extrusion at the lower half of the holder is also used to limit the tilting of the flexible holder.

Chapter 6

Electronics

6.1 RF resonator

As has been discussed in Chap. 3, about 70 V to 100 V RF voltage at 40 MHz will be needed to provide the necessary radial confinement to the ions. Supplying such high voltages from outside the cryostat is problematic, due to the Joule dissipations and noise pickups on the long feedthroughs. The solution is therefore supplying small amount of RF power from outside the cryostat via the feedthroughs, while amplifying the RF voltage as close to the trap as possible. A resonator with high Q value not only provides large amplification of the RF voltage at the resonance frequency, but also filters out other frequency components by its narrow passband, therefore reduces the noises injected to the experimental system. To provide the necessary RF voltage for the new trap, I have designed, built and tested a helical resonator similar to [33], for the RF frequency needed by the new trap.

6.1.1 Design

Helical resonators can provide (unloaded) Q values from several hundreds to even higher than 40000 [34], and also allows the impedance matching between the RF source and the ion trap [35, 36]. These attributes make them important devices for ion-trapping systems.

Since the helical resonator is going to be installed in our cryostat, we have more requirements for it. First of all, for better Q value, the material should have low resistivity. For this reason, oxygen-free high conductivity (OFHC) copper is used to build the metal parts of the resonator.Second, the size of the resonator must fit our cryostat. This forbids the over-sized designs. Since the optimal size of the resonator shield goes bigger as the desired resonance frequency goes down, I went for a design with sub-optimal Q value.

The design is based on the equations given by [35]. The Mathematica script

Length of shield	60 mm
Diameter of shield	45 mm
Diameter of helix	24.75 mm
Length of helix	37.125 mm
Number of turns	13.4056
Diameter of wire	1.385 mm
Pitch of helix	2.769 mm
Characteristic impedance	694.6Ω
Unloaded frequency	80 MHz
Unloaded Q	792.91
Loaded frequency	40.8 MHz

Table 6.1: Parameters for the 40 MHz resonator

which encodes these equations and converts the metric units into SI units written by Florian Leupold is used to ease the calculation. There are only two free parameters in this design process, which are the length of the shield, and the unloaded resonance frequency. The loaded resonance frequency depends on these two parameters, and also on the capacitive load of the resonator, which we don't know as *a priori*, so we can only use an estimated value in the designing phase. In the design, one has to adjust these two free parameters to tune the loaded central frequency to the desired value, and maximize the Q value.

Limited by the size of cryostat, I set the length of the shield 60 mm, which is the same as [33]. Estimating the capacitive load to be 6 pF, the unloaded resonance frequency which renders the loaded central frequency to be 40 MHz is 80 MHz. Then the other parameters for the helical resonator calculated according to [35] are summarized in Table. 6.1.

In practice, I did not find suppliers providing OFHC copper wires of 1.385 mm diameter, which is the optimal diameter for the helix, as shown in Table. 6.1. So the 1.50 mm diameter one was ordered from *Advent Research Materials* and used as a replacement.

6.1.2 Measurement

After this helical resonator was produced by the workshop, I did the measurements to characterize its resonance frequency and Q value.

For this measurement, I used a network analyzer to measure the reflected power spectrum of the resonator. When impedance matched, the power reflection rate at the resonance frequency should be 0, namely all the power is transmitted through the resonator. As the first step, different in-coupling coils were made and tested to match the impedance of RF source with the unloaded resonator. When the power reflection rate was tuned to no bigger

than 1% at the dip of the reflected power spectrum, the unloaded resonance frequency and Q value were noted:

$$\begin{aligned} f_c &= 68.465\,\text{MHz}, \\ \Delta f &= 68.520 - 68.415 = 0.105\,\text{MHz}, \\ Q &= \frac{f_c}{\Delta f} = 652, \end{aligned}$$

where Δf is the full width at half maximum (FWHM) of the power reflection spectrum. The reason that this resonance frequency differs from the designed value in Table. 6.1 should mainly be due to the copper wire used with different diameter than the designed value, which changes the inductance of this resonator. The measured Q value is smaller than the design, which can be due to the imperfect impedance matching, and the resistance from the connection of the SMA cable to the resonator input.

Since the capacitive load from the trap was not known as designed, I also characterized the resonance frequency and Q value of this resonator against different capacitive load, from which we can learn the rough range of capacitive loads which this resonator is suitable to work for. Here I connected ceramic capacitors of various values from 1 pF to 20 pF across the resonator output and the grounded shield. The in-coupling coil was adjusted for each capacitance value, to make the power reflection rate no bigger than 10% at the resonance frequency (for most of the capacitance values, smaller than 2.5%). The resonance frequency and Q value were measured in the same way by inspecting the power reflection spectrum using the network analyser. The results are shown in Fig. 6.1, where each data point was measured for 5 different capacitors with the same value, therefore the tolerance of the capacitance and the uncertainty coming from the contacts are reflected by the error bars.

From this measurement we can see that both the Q value and the resonance frequency drop as the load capacitance increases. The relatively poor impedance matching for 3 pF and 6 pF explains the two dips in the Q profile at these two capacitance values. As long as the total capacitive load does not exceed 15 pF, which should most likely be the case, we should not have problem using this resonator for our new SET, since the resonance frequency is still above 30 MHz, and the Q value is still decent.

6.2 RF-pickup circuit

According to Eq. 2.22, the pseudo-potential is determined by the RF field strength and the RF frequency. For a trap with fixed geometry, whose RF frequency is determined by the resonant frequency of the resonator, the pseudo-potential is then experimentally controlled by the RF voltage applied

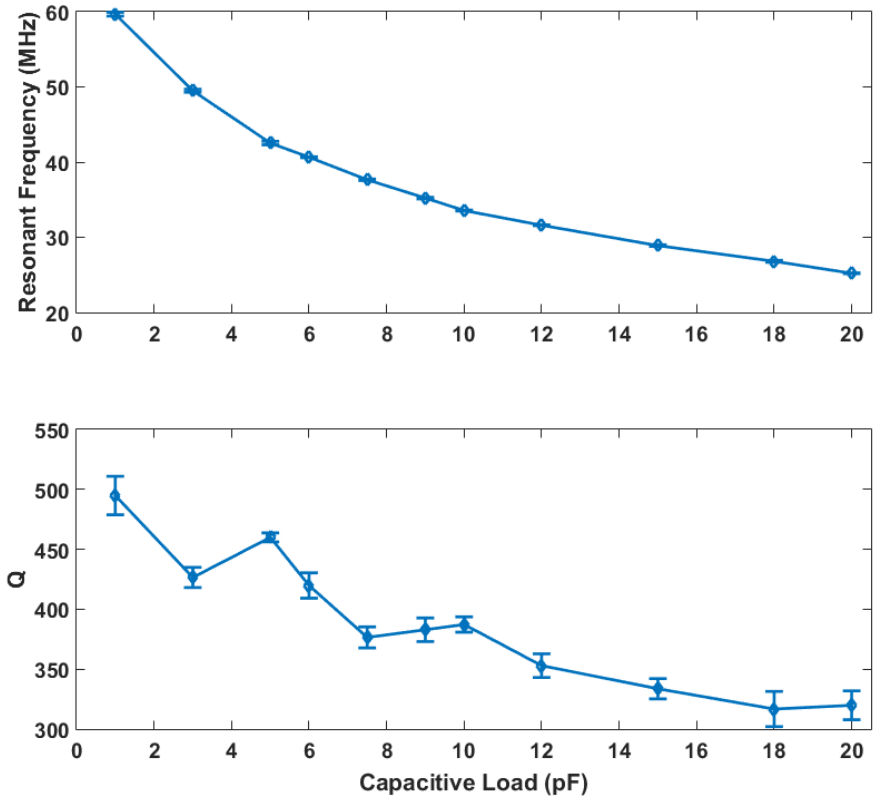


Figure 6.1: Measured resonant frequencies and Q values for different pure capacitive loads. The mean power refection rates at resonance frequency for these capacitive loads are respectively: 1.4%, 8.6%, 1.2%, 7.2%, 2.2%, 1.2%, 1.4%, 2.0%, 6.0%, 2.4%, 1.8%. The relatively poor impedance matching for 3 pF and 6 pF explains the two dips in the Q curve at these two points.

onto the trap. However, without a specially made measurement setup, we are not able to measure the actual RF voltage applied to the trap, but only have access to the RF power injected into the resonator. The reason is that, the voltage cannot be simply measured with a probe as is done for the DC, because for the RF, the measurement apparatus itself will change the working condition of the whole system, such as the impedance matching condition and the resonant frequency of the resonator.

In previous works this voltage has been measured with a capacitive voltage divider, like in [37]. For proper choices of the capacitor values, this method is able to measure the RF voltage on the trap, with minimal disturbance on the working condition of the system. However, the capacitive voltage divider does not stop noise from injecting into the system, which come from the measurement apparatus and are picked up by the long cable. Since this

measurement circuit is connected in parallel with the trap after the resonator, which can filter out the unwanted frequency components, the injected noise will directly influence the experiments with the ions. If we want to monitor the RF voltage on the trap in real time during the experiments, the noise injection has to be eliminated.

For these reasons, I have designed a RF-pickup circuit for monitoring the RF voltage in the future experiments, where I used a 1 pF as its front end which minimizes the disturbance to the system, and used an NE3510 n-channel heterojunction field effect transistor (FET) to prevent the noises from injecting into the trap.

6.2.1 Design

The schematic for this circuit is shown in Fig. 6.2.

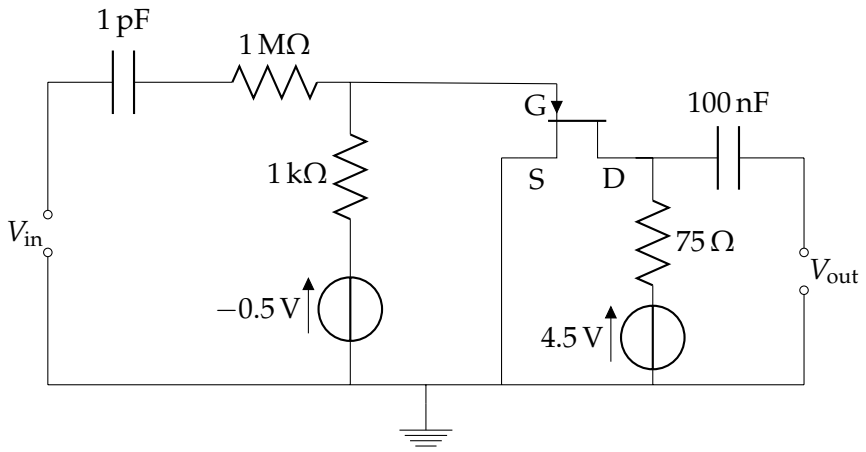


Figure 6.2: Schematic for the RF-pickup circuit. A 1 pF is used as the front end to minimize the capacitive load added to the resonator. A voltage divider formed by the 1 pF capacitor, 1 MΩ, and 1 kΩ resistors attenuates the RF signal amplitude by about 1000:1. An NE3510 n-channel FET allows the signal to go from Base to Drain, but forbids the noise from the feedthrough and measurement apparatus to inject to the trap. Voltage sources provide DC biasing for Gate and Drain of the transistor. The 75 Ω resistor makes the output impedance 50 Ω. A 100 nF capacitor passes the RF signal but prevents the impedance of feedthrough from changing the DC biasing condition of the transistor. The DC voltages from the two voltage sources are filtered by 100 nF resistors, which are not shown in this figure.

At the front end I am using a 1 pF capacitor. Therefore the total capacitance of this circuit seen from the input port is $\leq$ 1 pF, which will minimally shift the resonant frequency of the resonator, and barely changes the matched impedance of the resonator loaded with the trap. Since the RF voltage we are going to work with is $\approx$100 V as discussed in Sec. 3.2, and the AC signal amplitude at the FET gate should not exceed $\sim$0.1 V so that the small-signal model is valid for it, I have made a 1000:1 voltage divider with one 1 MΩ

resistor and one 1 kΩ resistor. For RF frequencies in the order of tens of MHz, the impedance of the 1 pF capacitor can be neglected comparing to the 1 MΩ after it. Here I am using resistive voltage divider because the 1 kΩ resistor is also used to DC bias the FET Gate, thus cannot be replaced by a capacitor. A −0.5 V DC source provides the DC biasing for the Gate of the FET [1]. The DC voltage is filtered by a 100 nF capacitor, which is not shown in Fig. 6.2

The Source of the transistor is directly connected to the ground, while a 4.5 V DC biasing is applied to the Drain. The 75 Ω resistor allows the DC biasing for the Drain, and also makes the impedance seen from the output port of this circuit roughly 50 Ω. I selected this value by simulating this transistor in Agilent ADC with the model file provided by the manufacturer of this transistor. The simulation shows that under our biasing conditions, the effective resistance across the Drain and Source is about 150 Ω. A 75 Ω in parallel with it seen from the output port therefore makes the output impedance 50 Ω.

At the output port, a 100 nF capacitor passes the AC signal, but blocks the DC. This capacitor is necessary, because otherwise the 50 Ω impedance coming from the coaxial cable and the terminated measurement apparatus will change the designed DC biasing condition for the FET Drain.

An BNC connector is used as the output port of this RF-pickup circuit, which allows us to connect this board to the measurement apparatuses with BNC coaxial cable.

6.2.2 Testing for the design

After the PCB for this circuit was manufactured, I did a test to verify our understanding of this circuit was correct and the transistor worked as predicted.

To ease the test and save the need for RF amplifier, I removed the 1 MΩ resistor in Fig. 6.2 to get rid of the 1000:1 voltage attenuator, making it possible to test the circuit with an RF source only (SRS DS345 waveform generator used here). The rest in Fig. 6.2 was not changed. With input voltage on the order of tens of mV, the output waveforms were clean sinusoids, whose amplitude linearly depended on the input voltage level. The measured gain of the transistor at 40 MHz (≈4.3) was comparable to the simulation result (4.66), and

[1] After the PCB for this circuit has been made, I realized that I could use a resistor at the Source of the transistor, thus the transistor can bias itself with the current flowing through the Source, and the −0.5 V Gate biasing voltage would no longer be needed. This design saves one power supply, therefore saves on feedthrough if we want to integrate the RF-pickup circuit onto the Cryo-Electronic Board, so I will go for it in an updated version.

the difference could be explained by impedance matching issue[2]and the tolerance of the DC biasing voltages.

To test the noise isolation provided by this circuit, I have also connected the waveform generator (SRS DS345) to the output port of this circuit, and looked at the signal at the input port with an oscilloscope. On the oscilloscope I could see an almost constant voltage signal, with only ≈2 mV fluctuations. Then the output level of the waveform generator was increased, emulating the stronger noises. But even when the amplitude was increased to the waveform generator's maximum output level, 250 mV_{rms}, there was no visible change in the waveform displayed on the oscilloscope. I have done this test for 30 MHz, 20 MHz, 10 MHz, 1 MHz, 500 kHz, and 100 kHz signals, and the results were the same. The noise isolation effect of this RF-pickup circuit as designed is therefore confirmed.

Due to the impedance matching issue, the voltage attenuation rate of the whole RF-pickup circuit (with the 1000:1 voltage divider) should be calibrated for the frequency it is working at. For different RF voltage ranges, the voltage divider on this circuit can be modified to have the optimal result. For example, when the RF voltage is increased to ≈150 V, saturation of signal becomes visible. A voltage divider with bigger attenuation rate is therefore needed if we are going to work within such voltage range.

6.3 Cryogenic Digital-Analog-Converter

To generate the necessary DC voltages for the DC electrodes of a trap, multichannel Digital-Analog-Converters (DACs) are commonly used [38, 39]. For those DACs working outside the cryostat, to apply their output voltages onto the trap which is operated inside the cryostat, feedthroughs have to be used. As the ion trap scales up, there will be more electrodes and wires requiring DC voltage inputs, and therefore more feedthroughs are required. Although the use of DACs is a scalable way to satisfy the increasing demands for DC inputs, the cumbersome feedthroughs will eventually limit the number of electrodes on the trap. The stray inductance and capacitance on the feedthroughs and cables can also introduce noise to the DC signals [39]. One solution to this problem is to move the DACs into the cryostat, so that their output channels are directly connected to the trap via the PCB, and the need for the feedthroughs is saved.

Since no commercial DACs are characterized for our 4 K environment, but according to our experiences some commercial electronics will actually work

[2]I have seen frequency dependence of the measured gain, which oscillated up and down against the frequency. This was a signature of unmatched impedance, presumably due to the tracks on the PCB (mainly the one for the RF input), which were not specially designed for the RF.

in this temperature although the datasheet does not claim so [33], it is worth doing a test for various commercial DACs, to search for a cryo-compatible model.

6.3.1 Requirements for DACs

To be used as the DC voltage supplies for our ion trap, we have the following minimal technical requirements to the DACs:

- Resolution. The precise control of the ions' motional states requires DC voltages with high enough resolutions. For this reason, I only tested the DACs having ≥ 10 bit resolutions.
- Number of channels. To solve the scalability problem, the DAC should have multiple output channels. The DACs with more output channels are more favorable, but as a minimal requirement, I am looking at DACs with ≥ 2 channels.
- Output voltage range. When designing the trap, the DC voltage range was assumed to be -10 to 10 V. When selecting the DACs, this requirement is slightly relaxed since in principle amplifiers can be used. But I am still requiring the DAC to have bipolar output, which means it must be able to generate both negative and positive voltages.

6.3.2 DACs to be tested

I found only 4 manufactures who have DAC(s) fulfilling all the three requirements above: Analog Devices Inc, Maxim Integrated, Linear Technology, and Texas Instruments. Unable to test all the commercial DACs fulfilling those requirements, I assumed the DACs from the same manufacturer are produced with the same technology[3], and therefore it is enough just to test the model with the highest specifications in the above-mentioned three aspects from each manufacturer. With these criteria, 4 DACs from the 4 manufacturers were selected, as are listed in Table 6.2.

6.3.3 Testing setup

The very basic test for the cryo-compatibility of these DACs is powering on in room temperature, setting up a certain output level with the serial or parallel interface, cooling its temperature to 4 K, and checking if the set output lever remains. If the output level is not affected by the low temperature,

[3] In fact this might not be a good assumption. Later we have heard from Professor Reilly from The University of Sydney, that even the DACs with the same model but from different factories can be fabricated with different technologies. But without further knowledge about how to distinguishing them, tests based on this assumption was the best I could do then.

Manufacturer	Part Number	Resolution	Number of Channels	Max. Output range
Analog Devices	AD5370	16 bit	40	$\pm$10 V
Maxim Integrated	MAX5735	16 bit	32	$\pm$5 V
Linear Technology	LTC2668	16 bit	16	$\pm$10 V
Texas Instruments	DAC8728	16 bit	8	$\pm$16.5 V

Table 6.2: DACs selected for the cryo-compatibility test. Except for TI DAC8728 which is controlled by parallel interface, all three others are controlled by Serial Peripheral Interface (SPI).

then other voltage levels will be set from the interface, to test if the logic still works.

Given both the two tests have been passed, the cold-start test will be done, where the DAC is first powered off, and then powered on in the 4 K temperature, to check if everything still works. A DAC able to cold start is essentially usable in our system, and the influence of the cryo-temperature on the resolution, responding time, and other properties can be evaluated afterwards.

To do such tests, PCBs are needed for the connections of power supplies, serial or parallel interfaces and the DAC outputs. I have made the designs of the PCBs as simple as possible, in case the failure of components other than the DAC causes the failure of the whole circuit. To generate the control sequences, I used an Analog Discovery Kit. The outputs of the DACs were measured with an oscilloscope.

The 4 K environment was generated by liquid Helium, contained in dewars with a 50 mm opening. For easier handling, I fixed the circuit board onto a 1 m long PTFE tube with 40 mm diameter, and used this tube to push the circuit into the liquid Helium dewar or pull it out. 3 m band cables were used for the power, input and output connections to the testing circuit board.

6.3.4 Testing Result

When testing each DAC, I first made sure the chip functioned well at room temperature, i.e. correct output voltage levels could be set by the input control waveforms. Then I slowly pushed the chip deep down into the dewar, and waited for it to thermalize with the liquid Helium. When heat was transfered from the chip to the liquid Helium, I could see the Helium vaporized and flowed out of the opening of the dewar. When gas Helium stopped flowing out of the dewar, I assumed the chip was cooled down to 4 K[4], and noted down the behavior of it.

[4]There is another possible reason for this, which is that the dewar has become empty. I verified the dewar not being empty by putting the tube into the dewar again after the test

The testing result for the 4 DACs are as following:

- AD5370. No matter what the original setted output level was in room temperature, it dropped to the negative analog supply voltage ($-15\,\mathrm{V}$) when cooled down to 4 K, and stopped responding to the control waveforms. Cold start did not work.
- LTC2668. No matter what the original setted output level was at room temperature, it dropped to 0 V when cooled down to 4 K, and stopped responding to the control waveforms. Cold start did not work.
- TI DAC8728. The setted output voltage dropped to 0 V even before the chip thermalized to 4 K. Cold start did not work.
- MAX5735. The output level dropped to 0 V when cooled down to 4 K. Cold start did not work. The digital part of this DAC worked (at least to some extent) at 4 K, because the chip provided a data echo channel, where the input command word in the previous 32 clock cycles were clocked out, and by monitoring this channel I confirmed at least this data echo function worked fine.

It is a pity that no DAC is found working at 4 K. Compared to the fast switched tested in [33], DACs have more complicated internal logics, therefore higher failure chances. But we have still gained some knowledge by doing this test, for example the problems in the analog parts might be the main reason that those DACs fail at 4 K. The working digital part in MAX5735 is a promising signal. According to its datasheet, the fabrication technology of this DAC is BiCMOS, which is an advanced technology combining bipolar junctions with the standard CMOS. This somehow gives us a hint about the direction to go, and the technology to aim for. In the future, given better knowledge about how to select the candidate DACs, we should be able to find the proper commercial DACs and make them work in the cryostat.

was finished. Gas Helium coming out of the opening indicated the dewar was not empty during the test.

Chapter 7

Trap characterization

Basic electrical tests are necessary for the better understanding of this ion trap fabricated in a CMOS foundry. Since the small size of this trap forbids us from directly tapping any probes onto it, we need to wirebond it to a testing PCB which extends the wire-bonding pads to the pin connectors accessible by normal measurement apparatus. For this task, I first designed a testing PCB to which the trap can be wirebonded, and then did the connectivity check, and measured the capacitance across the RF electrodes and the ground planes, the loaded resonant frequency and Q-value for the RF resonator, and the RF breakdown voltage.

7.1 Testing PCB

To test the electrical properties of the trap, a testing PCB is needed, to which the trap can be wirebonded, and the bonding pads are extended to the pin connectors which are accessible by probe and voltage sources. For a PCB to be wirebondable, we need to select the proper surface finishing techniques. For example, the most widely used surface finishing technique for ordinary PCBs, Hot Air Solder Leveling (HASL), is neither Al-bondable nor Au-bondable.

For Al-wirebonding, which is relevant to our application, possible PCB finishing techniques include Immersion Gold(IAu), Immersion Silver(IAg), Electroless Nickel Immersion Gold (ENIG), and Electroless Nickel/Electroless Palladium/Immersion Gold (ENEPIG) [40]. Since we only need this PCB for basic electrical tests in room temperature, and do not care the magnetic properties of it, we want the fabrication of it to be as cost efficient and as fast as possible. Therefore we have chosen the ENIG technique, which is the most widely used and most well-developed PCB finishing technique among the above mentioned candidates.

To ease the wirebonding, the bonding pads on the PCB should be located as close to the trap as possible. However, to avoid contaminations of these bonding pads when gluing the trap onto the PCB, a controversial requirement is to keep distance from the bonding pads to the trap. To fulfill those two conflicting requirements, I designed a separate holder, on which the testing PCB is fixed with screws, and the trap is glued onto the 1.5 mm $\times$ 3.7 mm pedestal lying in the center (see Fig. 7.1(a)). In this way the trap is elevated slightly above the PCB surface by this central pedestal on the holder, so that the gluing is done in a different plane from the PCB surface, therefore chances that the epoxy contaminates the bonding pads are minimized.

The testing PCB is shown in Fig. 7.1(b). A 3 mm $\times$ 5 mm slot is cut on the testing PCB which allows the trap and the pedestal to go through. Surrounding this slot, there are the 36 bonding pads, which are to be connected to the 36 bonding pads on the trap. To shorten the needed boding wires, and make the wireboding easier, we want to pattern the bonding pads on this PCB as compact as possible. However, we need tracks to lead these wirebonding pads to the pin connectors at the PCB edges, but the tracks cannot be patterned too close to each other, limited by the PCB manufacturer's[1]technical requirement about the minimum clearance between them. To keep the bonding pads as compact as possible without violating the technical requirement for track clearance, I used vias of the smallest possible size (0.3048 mm) to route half of the tracks to the second layer of the PCB, therefor the space is most efficiently utilized.

Fig. 7.1(c) shows the assembly of the testing PCB, the PCB holder and the trap to be tested. Stycast 2850 FT epoxy is used to glue the trap onto the pedestal on the PCB holder. Fig. 7.2 shows the trap wirebonded to the testing PCB.

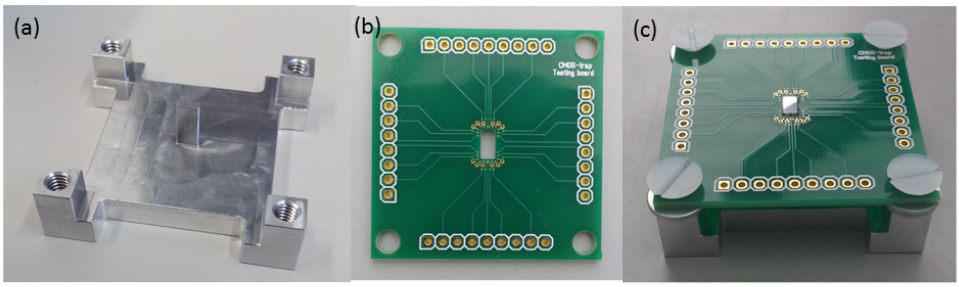


Figure 7.1: (a) The PCB holder made of Aluminium. At the center of it is the pedestal which lifts the trap above the PCB plane. (b) The testing PCB board, finished with ENIG. (c) The testing PCB, trap to be tested, and the PCB holder assembled together.

[1]Silver Circuits for this PCB

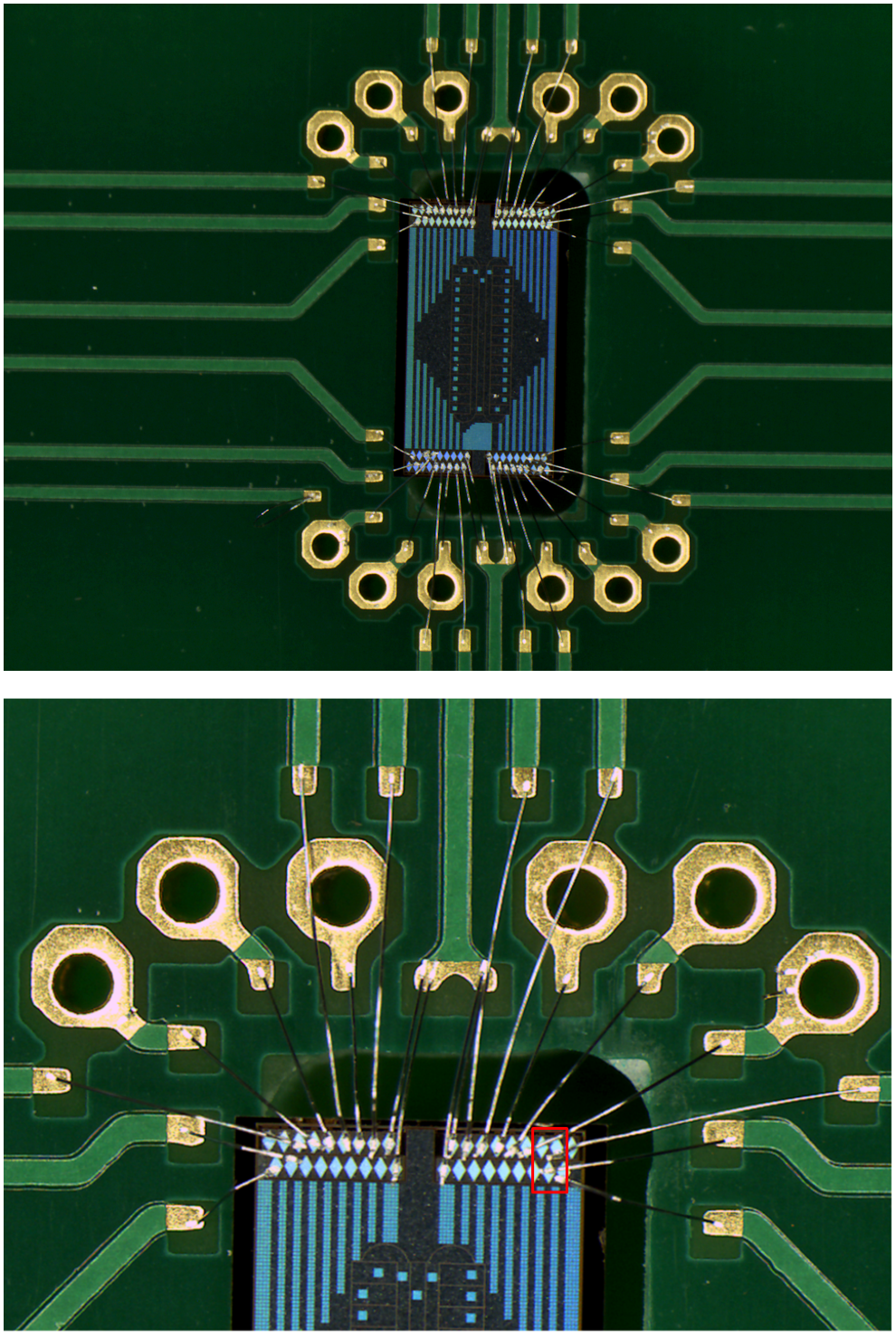


Figure 7.2: CMOS trap wirebonded to the testing PCB. Image taken under a light microscope. The lower picture zooms into the upper half of the chip, and the two bonding wires mistakingly connected to the same electrode is indicated by the red rectangle.

7.2 Connectivity check

After the trap is wirebonded to the testing PCB, I first did a connectivity check to make sure there are no short connections at the wirebonding pads, the tracks routed underneath the trap surface, and the adjacent electrodes. Connectivities between each pair of pins on the testing PCB are checked.

Except for the expected short between the pins for 'CMW' and 'CDC' pads, which are connected to the two ends of the central electrode to make it possible applying microwave to the trap, one short connection is found, between the 2nd and 3rd pins on the right-hand side of the breakout PCB. A careful check under light microscope reveals that this short in fact comes from the mistake that the two bonding wires are bonded to the pads for the same electrode, as indicated by red rectangle in Fig. 7.2. No short connections are detected for the rest of the pins.

This simple connectivity check to some extent confirms the quality and reliability of the CMOS technology[2]. There is no short connection coming from the neighboring bonding pads, adjacent electrodes, or the tracks and vias in the multi-layer structure.

7.3 Capacitance measurement

The capacitance between the RF electrodes and the RF grounded components (the ground plane as well as all DC electrodes) is an important parameter for our experiments, which affects the loaded resonant frequency and the Q value of the RF resonator.

The measurement is done with a *UNI-T UT39C Handheld Digital Multimeter*. At first, the capacitance between the RF electrodes and the ground plane is measured, by plugging the corresponding wires into the capacitance measurement slots on the multimeter. The returned capacitance value is 8 pF.

In the second step, I shorted all the DC electrodes to the chip ground plane, and repeated this measurement. Within the multimeter's sensitivity range, the returned measurement result is still 8 pF. This result is understandable, because on the chip, the RF electrodes and tacks have much bigger areas in parallel with the ground planes, than the surface area in in parallel with other DC electrodes.

The coupling between the RF track on the PCB with its neighboring tracks might also contribute to the capacitance value measured[3]. To evaluate this

[2]However there might also be other connectivity issues beyond short connections, such as open connections, which we cannot really tell yet. But in theory the shorting between adjacent electrodes should be the easiest failure mode.

[3]Note that there is no ground plane on this testing PCB. Otherwise we will expect more capacitance coming from the PCB.

effect, I repeated the same test for a bare PCB without trap wirebonded to it. All the pins except for the one meant for the RF are still shorted, and the capacitance between them and the RF pin is measured with the multimeter. This capacitance is only around 1 pF. Taken this correction into account, the capacitance on the trap between RF and ground is about 7 pF.

Depending on the size and the design of the final trap-carrier PCB, the total capacitance might be different from measurement result here. But as long as the size of the final PCB does not differ very much from the testing PCB used here, we do not expect the eventual capacitance to change much.

7.4 Loaded resonant frequency and Q-value of RF resonator

With the capacitance between RF and ground measured, we measured the resonant frequency and Q-value of the RF resonator, with the testing PCB loaded to it. This is an emulation of our real experimental system, with which we can have a rough estimation of the RF frequency we will actually be working at, and the actual voltage magnification of the resonator.

First the testing PCB with the trap wirebonded to is connected to the resonator. The wire leading to RF electrodes is winded onto the output of the resonator, and another wire which shorts the ground plane and all DC electrodes is fixed to the shield of the resonator, the ground of it. A network analyzer is used to measure the power reflection rate on the input port of the resonator.

At first, I made and tested different in-coupling coils for the resonator to eventually tune the reflection rate at resonant frequency to less than 1%. The resonant frequency and the Q-value is then noted:

$$\begin{aligned} f_c &= 33.8\,\text{MHz}, \\ \Delta f &= 34.10 - 33.51 = 0.59\,\text{MHz}, \\ Q &= \frac{f_c}{\Delta f} = 57.28. \end{aligned}$$

This resonant frequency roughly fits the curve in Fig. 6.1, where I characterized the resonant frequency against different capacitive loads. It is likely that there is an additional 1$\sim$2 pF capacitance coming from the wire and the connection, increasing the total capacitive load of the resonator to about 10 pF. However the Q-value of the loaded resonator is much smaller than what is characterized for purely capacitive loads as shown in Fig. 6.1 (57.28 vs 382.86). This indicates that the trap together with the PCB should not be a purely capacitive load. The resistance and/or the inductance of it signifi-

cantly degrades the Q-value of the resonator. Presumably this degradation is because of the non-negligible resistance coming from the wire-bonding.

In the next step, I connected the RF-pickup board to the resonator as well, in parallel with the trap. Since the capacitive load is increased, I remade the in-coupling coil for the resonator to adjust the reflection rate at resonant frequency to less than 1% again. The resonant frequency and Q-value of the loaded resonator is then shifted to:

$$\begin{aligned} f_c &= 30.855\ \text{MHz}, \\ \Delta f &= 31.148 - 30.578 = 0.57\,\text{MHz}, \\ Q &= \frac{f_c}{\Delta f} = 54.13. \end{aligned}$$

This shift can be well-understood, since there is another $1-2\,\text{pF}$ capacitance coming from the RF-pickup board, which lowers the resonant frequency as is characterized in Fig. 6.1.

7.5 RF breakdown voltage

The RF breakdown voltage of the trap is also of great interest to us, which determines how much voltage we can apply to the RF electrodes in the future experiments, and ultimately limits the strength of the radial confinement we can get from the trap.

For this measurement, in addition to the RF resonator as voltage amplifier, we have used another 47 dB RF amplifier to provide the high RF voltage necessary to break down the RF electrodes. A *TTi TGR1040* signal generator was used to generate the RF signal at the resonant frequency of resonator.

We then calibrated the voltage gain of the RF-pickup circuit at this frequency and used it to monitor the RF voltage applied to the trap. The calibration procedures were as following. We first set the output of the RF source to a certain level, and the frequency to the resonant frequency of the resonator. We then calibrated this output voltage by connecting the output to a 50 Ω terminated input port of the oscilloscope, with BNC cable. A 0.9 pF capacitor was connected to the 10X attenuated probe of the oscilloscope, which has a 10 MΩ resistance and a 16 pF capacitance, and therefore is not 50 Ω terminated. Afterwards, we terminated the output of the RF source with a 50 Ω terminator connected via a T-form symmetric BNC connector, and tapped the probe together with that 0.9 pF capacitor to the 50 Ω terminated output. The voltage value displaced on the oscilloscope was then noted down. By comparing this value with the true output voltage of the RF source we just measured, the voltage attenuation rate of this modified probe was known. We could therefore use this calibrated and modified probe to measure the

true input voltage of the RF-pickup board. Thanks to the 0.9 pF capacitor connected to the probe, tapping this probe onto the RF-pickup board input would barely change the impedance matching condition, so that it is not changing the working condition of the RF-pickup board. By comparing the output voltage of the RF-pickup board to the input voltage measured and derived from the calibrated probe, the gain of the RF-pickup board for this frequency was calibrated.

When doing this measurement, at first too much voltage (> 800 V_{peak}) was accidentally applied onto the trap. This broke down the RF electrodes immediately, and the wirebonding pads for the RF were also broken, as can be seen from Fig. 7.4.

Fortunately, another connectivity check showed that the DC electrodes were not broken (no short connections between each pair of the DC electrodes, nor between the DC electrodes to the ground plane). Therefore it was still possible to characterize the RF breakdown voltage with the DC electrodes. For this test, we then shorted the 15 DC electrodes (the lower 15 in Fig. 7.4) and used them as a new, big RF electrode. With this new RF electrode connected to the resonator, the resonant frequency was shifted to 13.585 MHz, because the capacitive load became higher due to the bigger surface area of the DC electrodes in parallel to the ground plane. We then built a new in-coupling coil for the RF resonator to improve the power transmission efficiency.

With the new setup, we increased the input power of the resonator from 13 dBm with 1 dBm step size, and monitored the output voltage applied to the trap using the RF pickup circuit (Fig. 7.3). The output voltage signal disappeared when the input power level increased to 38 dBm. The output did not reappear when the input power was reduced back to the previous level. This was an indication that the chip has been broken down. From Fig. 7.3 we can learn that the trap can withstand at least 182.6 V_{rms} RF voltage, which corresponds to 258.3 V_{peak} voltage.

Note that we have observed the transistor in the RF-pickup circuit being saturated when the input level was higher than 29 dBm. The saturation got severer as the input level went higher. So the 258.3 V_{peak} breakdown voltage must be an underestimation of the actual breakdown voltage, because the voltage gain from RF-pickup circuit must be lower than its normal value when saturated.

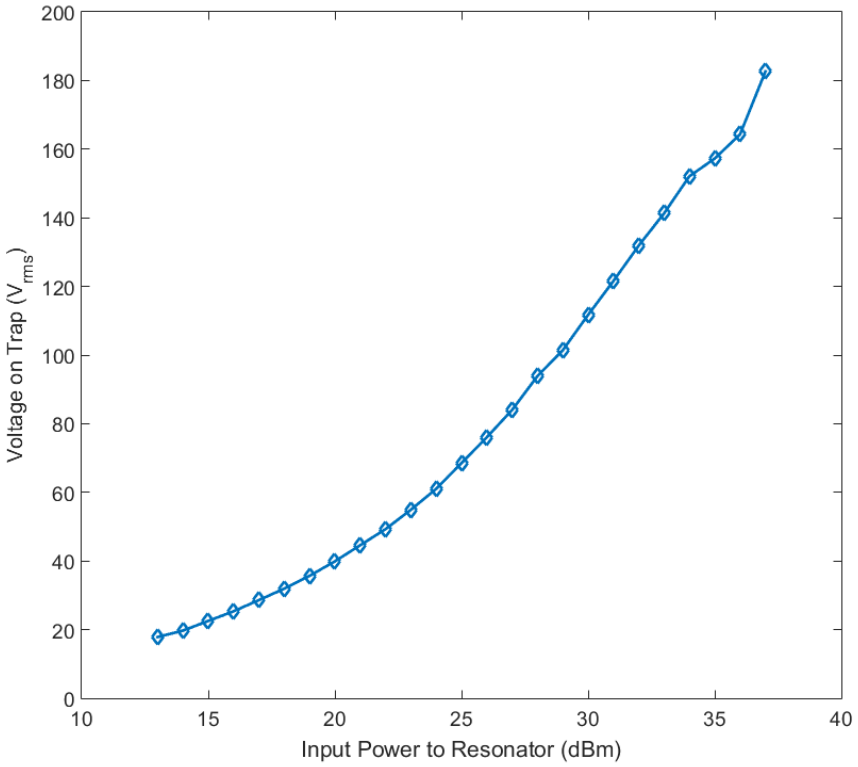


Figure 7.3: RF voltage applied to the trap against input power of the resonator. The voltages are measured with the calibrated RF-pickup board. The input power is known the output level set for the RF source, plus the 47 dBm gain of the RF amplifier.

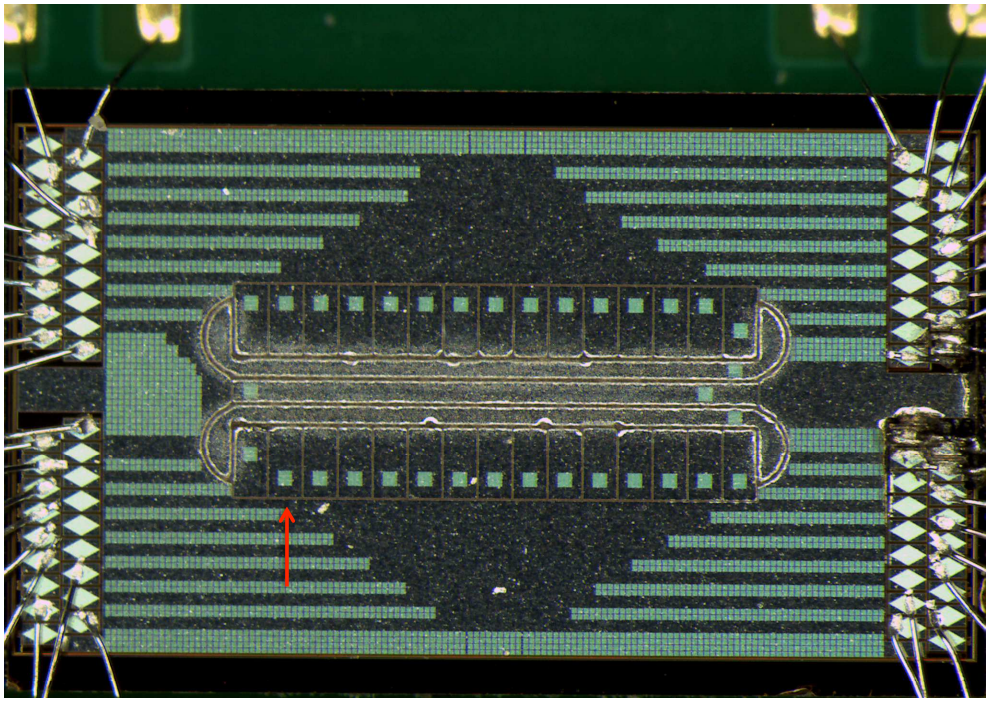


Figure 7.4: Trap brokendown by high RF voltage. Picture taken under light microscope. The RF electrodes were broken due to a $570 V_{\text{rms}}, 31\,\text{MHz}$ RF voltage mistakingly applied. Then the lower 15 DC electrodes are shorted to act as an effectively new 'RF' electrode. RF voltages at the new resonant frequency, $13.585\,\text{MHz}$, are applied to measure the breakdown of this new 'RF' electrode. Breaking-down occurred at about $180 V_{\text{rms}}$. After the breaking down, connectivity check was done for the 15 electrodes individually, and only one short connection was detected, which is indicated by the red arrow.

Chapter 8

Outlook

In this work, a new SET was fabricated with commercial CMOS technology, which has proved to be scalable in the VLSI industry, and is the building block for classical computers. The successful introduction of this technology to trapped-ion systems opens a promising way to scale up the trapped-ion quantum information processors to more qubits. After gaining more experience about this CMOS fabricated SET by evaluating its performance with experiments, we might consider designing bigger and more complicated SETs with T-junctions or cross-junctions, with which we can study the ion transportation over such junctions. Successful experiments on such kind of transportation will be a big step towards the quantum computer with the QCCD architecture [5], and this SET with junctions and the defined memory and interaction regions will become a prototype of scalable quantum computer, provided we are able to do quantum gates and the transportations with high fidelity. From purely technical points of view, we should already have no problems realizing such SETs with the same CMOS technology we are using here.

On this CMOS fabricated trap, I have made use of the multiple metal layers to route the tracks in a layer underneath the trap electrodes, and used vias to connect the tracks to the corresponding electrodes. By doing this, we have gained more flexibility in patterning the trap electrodes. This scheme has also made the realization of spatially isolated, 'island' like electrodes possible, which otherwise cannot get electrically connected. Therefore, in the future generation of the CMOS fabricated traps, we can consider segmenting the central DC electrode as well, which should provide us better control over the ions' motion when doing the ion transportation experiments.

The segmented central DC electrodes could also be very helpful for transportation experiments over the T or cross junctions, at the centers of which it might be harder to control the ion's motion using the segmented outer DC electrodes, as the ion-electrode distance to the outer electrodes is big-

ger there. If we can realize the 'bang-bang' diabetic transportation with fast switches [38] on the segmented central DC electrode, the transportation of the ion over the junctions could be done by simply combining two such 'bang-bang' transportations, as illustrated in Fig. 8.1. The 'bang-bang' transportation from/to the center of the junction can still be tricky, as the ion might have velocity components on both the x- and y- directions during the releasing-catching process, because at the center of the junction it's not well 'radially' confined by the RF[1]. But in principle this difficulty can be overcome by using the outer segmented DC electrodes to strengthen the radial confinement (x-confinement during y-transportation, and y-confinement during x-transportation. It will be anti-confining on z-direction due to Laplace condition), and allows the ion to move along only one direction.

In addition to its scalability, another feature of the CMOS technology is that it is also used to fabricate most of the ICs used in our experimental system, such as the fast switches and the DACs. This makes it tempting to integrate those necessary electronics onto the trap. The resulting chip would be beyond just an ion trap, but more like the quantum counterpart of the classical system on chip (SoC) IC, which is more scalable. The challenge we can foresee is the cryogenic temperature, as making cryo-compatible electronics is itself a highly non-trivial project for electrical engineers, which we have also tasted from the search of cryo-compatible DACs in this work. One possible solution is to use the more advanced CMOS technologies, such as the silicon-on-insulator (SOI) CMOS, the silicon-germanium bipolar plus CMOS (SiGe BiCMOS), or the SiGe:C BiCMOS. There are empirical experiences that these technologies will give ICs better cryo-compatibility than the standard CMOS technology we are now using.

Integrating photonics with the ion trap is also tempting. The practical difficulty is that most research works and the so far well-established technologies about the Si-based photonics are based on the 1310 nm to 1550 nm infrared band, which is widely used in fiber communication. Silicon itself has relatively higher absorption coefficient at our desired wavelengths as well. These are the challenges for integrating photonics with the SET.

Efforts on cryogenic electronics, even if not integrated with the trap, will also be beneficial by providing us better control for the experiments. This is another direction to work on in pursuit of a scalable trapped-ion quantum information processor.

Through-silicon via (TSV) is another thing we can explore in the future generations of CMOS fabricated SETs, which has already been used to realize a microfabricated SET [11]. The wirebonding pads can be saved, or at least

[1] Because at the junction center it's not well defined whether x or y is the 'radial' direction at all.

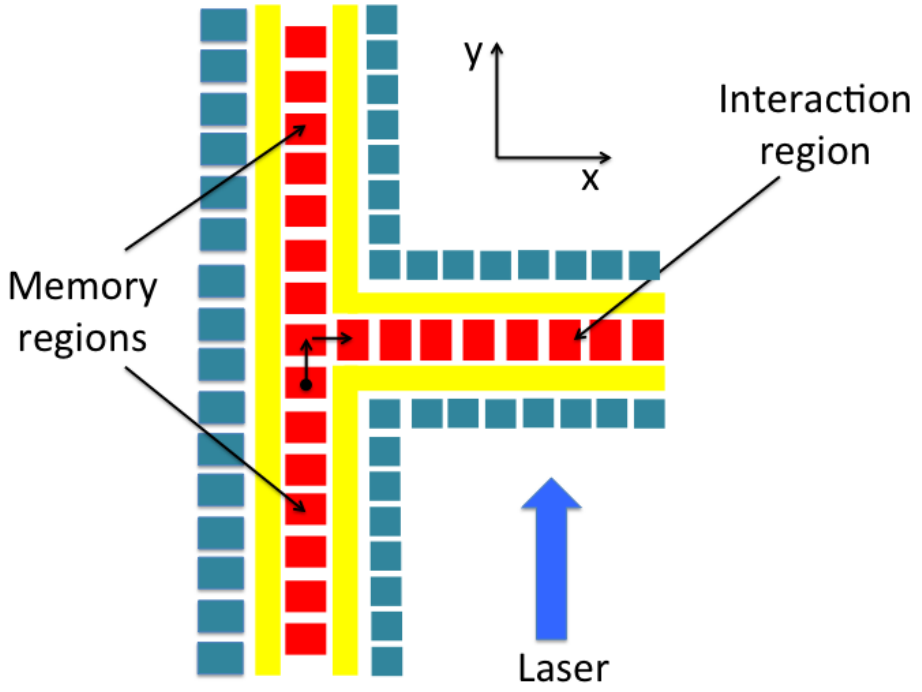


Figure 8.1: Sketch of a T-junction with segmented central DC electrodes. The segmented DC electrodes can be used to transport the ion across the junction. Especially, if we can realize the 'bang-bang' transportation with the segmented central DC electrodes, transporting the ion across the junction only needs two step: (a) releasing the ion from the 1st vertical electrode and catching it at the center electrode of the junction, (b) releasing the ion from the center electrode of the junction, and catching it at the 1st horizontal electrode. Realizing this 'bang-bang' scheme at the junction center can be tricky, because the ion might have velocity component on both the x- and y- directions. But in principle this can be overcome by using the other nearby outer segmented DC electrodes.

be moved to the backside of the trap by utilizing the TSVs. This change will give us unblocked laser accessibility on top of the trap. By making use of TSVs, ICs can be stacked on top of each other to form a '3D-IC'. This is an undergoing research area in microelectronics. If we could find suitable collaborators, it is possible to use such technology to stack two CMOS fabricated traps, and realize the bi-layer SET proposed in [41].

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