Tutorial

Advanced Modeling and Multi-Objective Optimization / Evaluation of SiC Converter Systems

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Outline

► Introduction
► Basic Multi-Objective Optimization Approach
► Component Models incl. Costs
► Converter Optimization / Evaluation – Example I
► Converter Optimization / Evaluation – Example II
► Conclusions
Introduction

Performance Trends
Performance Space
Pareto Front
Design Space
Power Electronics Converters
Performance Trends

Performance Indices
- Power Density \([\text{kW/dm}^3]\)
- Power per Unit Weight \([\text{kW/kg}]\)
- Relative Costs \([\text{kW/$}]\)
- Relative Losses \([\%]\)
- Failure Rate \([\text{h}^{-1}]\)

Environmental Impact...
- [kg\(_{Fe}\) / kW]
- [kg\(_{Cu}\) / kW]
- [kg\(_{Al}\) / kW]
- [cm\(^2\) Si / kW]

State-of-the-Art
Future
Costs
Time-to-Market
Losses
Weight
Volume
Failure Rate
► Performance Improvements (1)

- Power Density
  - Telecom Power Supply Modules: Typ. Factor 2 over 10 Years
Performance Improvements (2)

Inefficiency (Losses)... \[1 - \eta\]

Efficiency

- PV Inverters: Typ. Loss Red. of Typ. Factor 2 over 5 Years
Performance Improvements (3)

- Costs
  - Importance of Economy of Scale
Performance Improvements (4)

Costs

- Automotive: Typ. 10% / a
- Economy of Scale!

Source: PCIM 2013
**Design Challenge**

- Mutual Coupling of Performance Indices $\rightarrow$ Trade-Off Analysis (!)

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For Optimized Systems Several Performance Indices Cannot be Improved Simultaneously
Design Challenge

- Mutual Coupling of Performance Indices → Trade-Off Analysis (!)

For Optimized Systems Several Performance Indices Cannot be Improved Simultaneously
Design for Specific Performance Profiles / Trade-Offs Dependent on Application

Graphical Representation of Performance

- Domestic Applications
- Laboratory Applications
- Information & Communication Industry
- Aerospace Applications
Mutual Coupling of Performances (1)

- Experimental Exploration of the Power Density Improvement of a Three-Phase PFC Rectifier System with Increasing Switching Frequency

- Graph showing power density ($\rho$) vs. switching frequency ($f_P$) for different switch frequencies and power densities:
  - $f_P = 50$ kHz, $\rho = 3$ kW/dm$^3$
  - $f_P = 72$ kHz, $\rho = 4.6$ kW/dm$^3$
  - $f_P = 250$ kHz, $\rho = 10$ kW/dm$^3$
  - $f_P = 1$ MHz, $\rho = 14.1$ kW/dm$^3$
Mutual Coupling of Performances (2)

- Experimental Exploration of the Power Density Improvement of a Three-Phase PFC Rectifier System with Increasing Switching Frequency

\[ f_P = 50 \text{ kHz} \]
\[ \rho = 3 \text{ kW/dm}^3 \]

\[ f_P = 72 \text{ kHz} \]
\[ \rho = 4.6 \text{ kW/dm}^3 \]

\[ f_P = 250 \text{ kHz} \]
\[ \rho = 10 \text{ kW/dm}^3 \]

\[ f_P = 1 \text{ MHz} \]
\[ \rho = 14.1 \text{ kW/dm}^3 \]

Consideration of a Single Performance Index is NOT Sufficient (!)
Mutual Coupling of Performances (3)

- Consideration of a Single Performance Index is NOT Sufficient (!)
- Trade-Off of Performances Must be Considered \(\rightarrow\) \(\eta\)-\(\rho\)-Performance Limit

\[
\begin{align*}
\eta &= \text{efficiency} \\
\rho &= \text{power density} \\
\end{align*}
\]

- \(f_p = 50\) kHz \(\rho = 3\) kW/dm\(^3\)
- \(f_p = 72\) kHz \(\rho = 4.6\) kW/dm\(^3\)
- \(f_p = 250\) kHz \(\rho = 10\) kW/dm\(^3\)
- \(f_p = 1\) MHz \(\rho = 14.1\) kW/dm\(^3\)
Example of $\eta$-$\rho$-Trade-Off (1)

- **1-$\Phi$ Boost-Type PFC Rectifier**

  - Si CoolMOS, 99m$\Omega$/600V
  - SiC Diodes, 10A/600V

$P_0=3.2\text{kW}$

$U_N=230\text{V}\pm10\%$

$U_0=365\text{V}$

$f_\rho=33\text{kHz} \pm 3\text{kHz}$

Two Interleaved
1.6kW Systems

$\star 99.2\% @ 1.1\text{kW/dm}^3$
Example of η-ρ-Trade-Off (2)

- 1-Φ Boost-Type PFC Rectifier
  - Si CoolMOS
  - SiC Diodes

\[ P_0 = 3.2\, \text{kW} \]
\[ U_N = 230\, \text{V} \pm 10\% \]
\[ U_0 = 400\, \text{V} \]

\[ f_P = 450\, \text{kHz} \pm 50\, \text{kHz} \]

Two Interleaved
1.6kW Systems

★ 5.5kW/dm³ @ 95.8%
Derivation of the $\eta - \rho$-Performance Characteristic

* Semiconductors / Heatsink
* Output Capacitor
* Inductor
Analysis of $\eta$-$\rho$-Performance Characteristic (1)

Specifications / Assumptions

- Rated Output Power $P_2$
- Const. Input Current Ripple $\Delta i_i$
- Const. Output Capacitance $C_0$ (Energy Storage)
- Const. $T_j$ of Power Semiconductors $\approx T_s$
- Def. Ambient Temperature $T_a$

Dependency of Component Losses / Volumes on Switching Frequency $f_p$

- Input Inductor
- Output Capacitor
- Semiconductors / Heatsink
Analysis of $\eta$-$\rho$-Performance Characteristic (2)

- **Input Inductor**
  \[ \Delta i \propto \frac{U_o}{L} T_P \rightarrow \frac{\Delta i}{I} \propto \frac{U_o}{L I} \frac{1}{f_P} \rightarrow LI \propto \frac{U_o}{\alpha_{\Delta i}} \frac{1}{f_P} \rightarrow LI^2 \propto \frac{U_o I}{\alpha_{\Delta i}} \frac{1}{f_P} \]

- **Inductor Power Density**
  \[ V_L \propto \frac{1}{2} LI^2 \propto \frac{P_o}{f_P} \rightarrow \rho_L = \frac{P_o}{V_L} \propto \frac{1}{f_P} \]

- **Relative Inductor Losses**
  \[ P_L = P_W + P_C \approx P_0 + k_L f_P^{\alpha_L} \rightarrow \varepsilon_L = \frac{P_L}{P_0} \propto (1 + k_L f_P^{\alpha_L}) \]

- **Output Capacitor**
  \[ V_C \propto \frac{1}{2} C U_O^2 = \text{const.} \rightarrow \rho_C = \frac{P_o}{V_C} = \text{const.} \quad P_C \approx 0 \quad \rightarrow \varepsilon_L \approx 0 \]
Analysis of $\eta$-$\rho$-Performance Characteristic (3)

- Semiconductors & Heatsink

  Relative Semiconductor Losses

  \[ P_S = P_C + P_P \approx P_C + k_P f_P \quad \rightarrow \quad \varepsilon_S = \frac{P_S}{P_O} \sim (1 + \kappa_P f_P) \]

  Heatsink Volume / "Power Density"

  \[ CSPI = \frac{G_{th}}{V_S} = \frac{P_S}{\Delta T_{s-a} V_S} \quad \rightarrow \quad \rho_S = \frac{P_O}{V_S} = \Delta T_{s-a} CSPI \frac{P_O}{P_S} = \Delta T_{s-a} CSPI \varepsilon_S^{-1} \]
Analysis of $\eta$-$\rho$-Performance Characteristic (4)

System Efficiency & Power Density in Dependency of $f_p$

- **Efficiency**

\[
\eta = \frac{P_O}{P_i} = \frac{P_i - (P_L + P_S)}{P_i} = 1 - \frac{(P_L + P_S)}{P_i} \approx 1 - \frac{(P_L + P_S)}{P_O} = 1 - (\varepsilon_L + \varepsilon_S)
\]

- **Power Density**

\[
\rho = \frac{P_O}{V} = \frac{P_O}{V_L + V_S + V_C} = \frac{1}{\frac{V_L}{P_O} + \frac{V_S}{P_O} + \frac{V_C}{P_O}} \rightarrow \\
\rho = (\rho_L^{-1} + \rho_C^{-1} + \rho_S^{-1})^{-1}
\]

- $f_p$ as Parameter of $\eta = \eta \{ \rho \}$ - Characteristic
Analysis of $\eta$-\(\rho\)-Performance Characteristic (5)

- Specific Design $\rightarrow$ Only $f_p$ as Variable Design Parameter
- Only the Consideration of All Possible Designs / Degrees of Freedom Clarifies the Absolute $\eta$-\(\rho\)-Performance Limit

$\star$ $f_p = 100\text{kHz}$
Determination of the $\eta$-$\rho$-Pareto Front

- **Comp.-Level Degrees of Freedom of the Design**
  - Core Geometry / Material
  - Single / Multiple Airgaps
  - Solid / Litz Wire, Foils
  - Winding Topology
  - Natural / Forced Conv. Cooling
  - Hard-/Soft-Switching
  - Si / SiC
  - etc.
  - etc.
  - etc.

- **System-Level Degrees of Freedom**
  - Circuit Topology
  - Modulation Scheme
  - etc.
  - etc.
  - etc.

- **Only $\eta$-$\rho$-Pareto Front Allows Comprehensive Comparison of Converter Concepts (!)**
Basic Multi-Objective Optimization Approach

Abstraction of Converter Design
Component / System Modeling
Design / Performance Space
Pareto Front
Abstraction of Power Converter Design

Performance Space
- Efficiency
- Power Density
- Costs
- Reliability
- etc.

Design Space
- Evaluation Formulas
- Lifetime Models
- Cost Models
- etc.

Components
- Power Semiconductor
- Interconnections
- Inductors, Transformer
- Capacitors
- Control Circuit
- etc.

Materials
- Semiconductor Material
- Conductor Material
- Magnetic Material
- Dielectric Material
- etc.

Mapping of Design Space into System Performance Space
Modeling and Multi-Objective Optimization of Converter Design

Specifications
\( V_1, V_0, P_0, \Delta V_0, \text{CISPR 11/22 A.B} \)

Converter Topology Modulation Scheme

Electric Power Circuit Model

Component Values, \( f_c \)

Capacitor Type
- Transformer / Inductor
  - Windings Geom.
  - Wire Type
  - Core Geom.
  - Core Type
- Loss Model
  - Min. Losses
  - \( B \leq B_s \)
  - \( T \leq T_{max} \)
  - \( V \leq V_{max} \)
- Capacitor Volume
- Capacitor Losses
- Transformer / Inductor Volume
- Power Losses

Semiconductor Type

Reluctance Model
- \( \Phi / \Phi_{max} \)

Thermal Model
- \( R_h \)
- \( T_C / T_W \)

Off-line Optimized Heat Sink
- EMI Filter Ind. Vol.

Total Converter Volume / Losses

Summation of Component Volumes and Losses

Minimum Losses or Volume

CM Noise Model

DM Noise Model

Off-line Optimized DM/CM Filter Topology

Filter Capacitor Type
- Geometry
- Material

Filter Inductor

ETH zürich
Multi-Objective Converter Design Optimization

- *Pareto Front* - Limit of Feasible Performance Space

$$
\begin{align*}
\overrightarrow{k} &= (k_1, k_2, \ldots, k_i) \\
\overrightarrow{x} &= (x_1, x_2, \ldots, x_n) \\
\mathbf{p}_i &= f_i(\overrightarrow{x}, \overrightarrow{k}) \\
g_k &= (\overrightarrow{x}, \overrightarrow{k}, \overrightarrow{r}) = 0 \\
h_j &= (\overrightarrow{x}, \overrightarrow{k}, \overrightarrow{r}) \geq 0 \\
\overrightarrow{p} &= (p_1, p_2, \ldots, p_i) \\
\sum w_i f_i(\overrightarrow{x}, \overrightarrow{k}) &= \sum w_i p_i \rightarrow \text{Max}
\end{align*}
$$
Technology Sensitivity Analysis Based on $\eta$-$\rho$-Pareto Front

- Sensitivity to Technology Advancements
- Trade-off Analysis

![Diagram showing design space and performance space with the concept of sensitivity analysis based on the $\eta$-$\rho$-Pareto front.]
Converter Performance Evaluation Based on \(\eta\)-\(\rho\)-Pareto Front

- **Performance Indicator**

\[
\tan \alpha_D = \frac{1 - \eta_D}{\rho_D}
\]

- **Design Space Diversity**

Design Variables & Constraints Related to Two Adjacent Points of the Pareto Front
**Converter Performance Evaluation Based on $\eta$-$\rho$-Pareto Front**

- **Triple-Interleaved TCM Rectifier (33kHz)**
- **Double-Interleaved Double-Boost CCM Rectifier (33kHz)**
- **Triple-Interleaved TCM Rectifier (56kHz)**
- **Double-Interleaved Double-Boost CCM Rectifier (450kHz)**

![Diagram showing efficiency vs. power density with points for different converter configurations.](image-url)
3D-Performance Space Including Costs
Industry Perspective

Priorities

1. Costs
2. Costs
3. Costs
4. Robustness
5. Power Density
6. Efficiency

Modularity / Scalability / Ease of Integration into Systems / etc.

Basic Discrepancy (!)

* Most Important Industry Figure “Unknown” to Univ.
* Costs Not Considered in Applic.-Oriented Research
Requirement for Quantitative Cost Models

Advantages / Competitiveness of SiC can only be revealed considering full system costs.

- Considering only volumes is insufficient
- Initial / Manufacturing Costs
- Life Cycle Costs
- Complexity / Reliability
- Functionality

\[ \eta_{\text{SiC}} > \eta_{\text{Si}}, \quad f_{\text{sw, SiC}} > f_{\text{sw, Si}} \]

State-of-the-Art → Si IGBTs

Advanced → SiC MOSFETs
Converter Performance Evaluation Based on $\eta$-$\rho$-$\sigma$-Pareto Surface

- $\sigma$: kW/$
Converter Performance Evaluation Based on $\eta$-$\rho$-$\sigma$-Pareto Surface

- Maximum $\sigma$ [kW/$\$], Related Efficiency and Power Density
- Definition of "Technology Node" $\rightarrow (\eta^*, \rho^*, \sigma^*, f_P^*)$
Modeling of Components

- Efficiency
- Power Density
- Costs
Power Semiconductors and Cooling Systems

* Cond./Switching Loss Models
* Thermal Models
* Cost Models
Modeling Tasks and Design Variables

- **Design Routine**

  System Design Variables:
  - $f_{sw}$
  - Component Values $L, C$
  - Modulation Scheme

  System Model

  ![Diagram of System Model]

  Comp. Stress:
  - $i(t), u(t)$

  Loss Models:
  - Switching Losses
  - Conduction Losses
  - Fan Losses
  - Gate Driver Losses

  Thermal Models

  $T_j < T_{\text{max}}$

  Cost Models

  Store Design:
  - Losses
  - Volumes
  - Costs

- **Thermal Model**

  ![Diagram of Thermal Model]

  Component Design Variables:
  - Semiconductor Type
  - \# parallel / $A_{\text{chip}}$
  - Cooling System / $R_{\text{th,hea}}$
    - Sink Dimensions
    - Sink Material
    - Fan Type
    - \# Fans

  $P_{SC}(T_j)$
## Conduction Losses

### MOSFET Conduction Losses

\[ P_{\text{cond}}(i(t), T_j) = R_{ds,\text{on}}(i(t), T_j) \cdot i(t)^2 \]

- **Take from Data Sheet**

**Conditions:**
- \( V_{DS} = 20 \text{ V} \)
- \( I_D < 200 \mu\text{A} \)

Source: CREE
Switching Losses

MOSFET Switching Losses

\[
P_{sw} = \frac{1}{T} \sum_i \left[ E_{on}(I_{on,i}, V_{on,i}, T_j) + E_{off}(I_{off,i}, V_{off,i}, T_j) \right]
\]

Measurement Results

- Layout-Dependent / Measurements Required
# Semiconductor Costs

- **Source of Cost Data**
  - Distributors
  - Better: Manufacturer Data @ MOQ = const.

- **Cost Model**

\[
\sum_{SC} = \sum_{pack} + \sigma_{\text{chip}} \cdot A_{\text{chip}}
\]

---

**Fitted Manufacturer Data for MOQ = 50k**

<table>
<thead>
<tr>
<th>Chip technology</th>
<th>Si T&amp;FS IGBT</th>
<th>Si PIN diode</th>
<th>Si CoolMos CS7</th>
<th>SiC Schottky diode</th>
<th>SiC MOSFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \sigma_{600 \text{V}} ) ( \text{chip,}\text{cm}^2 )</td>
<td>5.52</td>
<td>2.46</td>
<td>30.27</td>
<td>46.24</td>
<td>61.14</td>
</tr>
<tr>
<td>( \sigma_{1200 \text{V}} ) ( \text{chip,}\text{cm}^2 )</td>
<td>6.57</td>
<td>4.46</td>
<td></td>
<td>86.47</td>
<td>72.01</td>
</tr>
<tr>
<td>Package type</td>
<td>TO-247-3</td>
<td>SOT-227</td>
<td>Module (23.2 cm(^2))</td>
<td>Module (29.9 cm(^2))</td>
<td>Module (37.6 cm(^2))</td>
</tr>
<tr>
<td>( \Sigma_{\text{pack,}\text{unit}} ) ( \text{cm}^2 )</td>
<td>0.55</td>
<td>8.10</td>
<td>7.62</td>
<td>10.01</td>
<td>15.06</td>
</tr>
</tbody>
</table>

MOQ ... Minimum Order Quantity
Cooling System Modeling

- Geometry, Fans
  - Heat Sink Dimensions
  - Heat Sink Material
  - Fan Type
  - # of Fans

- Fluid Dynamics Models
- Thermodynamics Models

- Experimental Verification

![Graph showing thermal resistance vs cooling system number]
Cooling System Costs

- Fan Costs
  - Distributors
  - Better: Manufacturer Data @ MOQ = const.

- Cost Model for Heat Sinks
  \[ \Sigma_{\text{sink}} = \Sigma_{\text{sink}}^{\text{fc}} + \sigma_{\text{sink}} \cdot V_{\text{sink}} \]
  - Based on Fitted Manufacturer Data

---

<table>
<thead>
<tr>
<th>Heatsink type</th>
<th>Extruded</th>
<th>Extrud./anodized</th>
<th>Hollow-fin</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \sigma_{\text{sink},x} ) (( \text{dm}^3 ))</td>
<td>7.69</td>
<td>9.30</td>
<td>11.94</td>
</tr>
<tr>
<td>( \Sigma_{\text{sink},x} ) (( \text{Unit} ))</td>
<td>0.23</td>
<td>0.25</td>
<td>0.17</td>
</tr>
</tbody>
</table>
Magnetic Components

* Core/Winding Loss Models
* Reluctance Models
* Thermal Models
* Cost Models
Modeling Tasks and Design Variables

Design Routine

System Design Variables:
- $J_{SW}$
- Component Values $L, C$
- Modulation Scheme

Comp. Stress:
$$\sum_{i=1}^{n} I_{(n)} \times i(t), u(t)$$

Relductance Models

Loss Models:
- Core Losses
- Winding Losses

Component Design Variables:
- Core
  - Type (E-, U-, Toroid,...)
  - Dimensions
  - # Air Gaps
  - # Stacked Cores
  - Material
- Coil Former
  - Dimensions
  - Material
- Winding
  - Type (Round, Litz,...)
  - Dimensions
  - # Turns
  - Material

Store Design:
- Losses
- Volumes
- Costs

www.pack-feindraehte.de  
www.jiricek.de
### Core Losses

- **Improved\(^2\) Steinmetz Equation**

\[
P_{\text{core}} = V_{\text{core}} \cdot \frac{1}{T} \cdot \sum_{i} k_i \Delta T_i^{1-\alpha_i} |\Delta B_i|^{\beta_i}
\]

- **Improvement (1):** Arbitrary Waveforms
- **Improvement (2):** Operating Point-Dependent Parameters

- Requires Extensive Measurements
- Sweeps: \(f, B_{\text{ac}}, B_{\text{dc}}, T_{\text{core}}, l_{\text{ag}}\)
Winding Losses

\[ P_{\text{wdg}} = R_{dc}(T_{\text{wdg}}) \cdot \sum_{n} \left\{ F_{\text{skin}}(f_n, T_{\text{wdg}}) + G_{\text{prox}}(f_n, T_{\text{wdg}}) \cdot \overline{H}_{\text{ext},(n)}^2 \right\} \cdot I_{(n)}^2 \]

- Skin and Proximity Effects Contribute to Winding Losses
- Frequency-, Temperature- and Geometry-Dependency
- Analytical Formulas for \( F_{\text{skin}}, G_{\text{prox}} \) and \( H_{\text{ext}} \) Available
Thermal Models

- 3D Equiv. Thermal Network

Winding: hot spot to surface

- Conduction
- Radiation
- Natural Convection

Core: hot spot to surface

- Significance
  - Avoid overheating
  - Improve loss calculation

- Heat Transfer Mechanisms
  - Conduction
  - Radiation
  - Natural Convection
Verification of Multi-Physics Models

- **Setup**

- **Test Inductors**

- **Loss Model Verification**

- **Thermal Model Verification**
Magnetics Costs

Model

\[ \Sigma_L = \frac{1}{GM} \left( \Sigma_{\text{core}} + \Sigma_{\text{wdg}} + \Sigma_{\text{lab}} \right) \]

\[ \Sigma_{\text{core}} = N_{\text{stack}} \cdot \Sigma_{\text{fc}}^{\text{core}} + \sigma_{\text{core}} W_{\text{core}} \]

\[ \Sigma_{\text{wdg}} = \Sigma_{\text{fc}}^{\text{wdg}} + \sigma_{\text{wdg}} W_{\text{wdg}} \]

\[ \Sigma_{\text{lab}} = \Sigma_{\text{fc}}^{\text{lab}} + \sigma_{\text{lab}} W_{\text{wdg}} \]

Example: Manufact. Data for Litz Wire for MOQ = 1 Metric Ton

Source of Data

- Core Manufacturers
- Conductor Manufacturers
- Suppliers of Magn. Components
Capacitors

* Loss Models
* Cost Models
Modeling Tasks & Design Variables

System Design Variables:
- $f_{sw}$
- Component Values $L$, $C$
- Modulation Scheme

System Model

Comp. Stress:
$$\sum_{n} i_{(n)}(t)$$

Component Design Variables:
- Capacitor Type
  (Film, Electrolytic,....)
- Rated Capacitance
- Rated Voltage
- # Parallel
- # Serial

$I_{rms} < I_{rms,max}$
$
\Delta V_{pp}^c < \Delta V_{pp,max}^c
$

No

Yes

Loss Models
Cost Models

Store Design:
Losses
Volumes
Costs
Capacitor Losses

Electrolytic Capacitor Losses

\[ P_C = \sum_{n} ESR(f_{(n)}, T_{amb}) \cdot \frac{1}{2} I^2_{(n)} \]

- Take from Data Sheet
**Capacitor Costs**

- **Cost Models**

  \[
  \Sigma_{Al-e} = b_{Al-e} V_r + c_{Al-e} C_r V_r^2 \\
  \Sigma_{film} = a_{film} + b_{film} V_r + c_{film} C_r
  \]

  Parameters Based on Fitted Data

- **Source of Cost Data**

  - Distributors
  - Better: Manufact. Data @ MOQ = const.

Fitted Manufact. Data for MOQ = 50k
Converter Optimization Example I

Isolated DC/DC Converter
Topologies/Modulation Schemes
Materials/Components
Optimization
η-ρ-σ-Pareto Surface
Hardware Prototype
Application

- Next Generation Residential Energy Management System

- Renewable Energy Sources, Local Storage Systems
- DC Distribution Bus
- Intelligent Load Management Algorithm
- Possible Element of Future Smart Grid System
- DC Microgrids Already Employed in Data Centers, Ships, Airplanes
Bidirectional Wide Input Voltage Range Isolated DC/DC Converter

Structure of DC Microgrid

- Universal DC/DC Converter
  - Bidirectional Power Flow
  - Galvanic Isolation
  - Wide Voltage Range
  - High Partial Load Efficiency

Universal DC/DC Converter

Advantages
- Reduced System Complexity
- Lower Overall Development Costs
- Economies of Scale
Converter Topologies

- Conv. 3-Level Dual Active Bridge (3L-DAB)

- Advanced 5-Level Dual Active Bridge (5L-DAB)
Modulation Schemes

■ 3-Level Dual Active Bridge

■ 5-Level Dual Active Bridge

\[ \Xi_{3LDAB} = (D_{1b}, D_{1b}, D_{2}, 0, \varphi_{12})^T \]

\[ \Xi_{5LDAB} = (D_{1a}, D_{1b}, D_{2}, \varphi_{ab}, \varphi_{12})^T \]

\[ \Xi^* = \text{arg min}_{\Xi} I_{ac1,\text{rms}}(n^*, L^*, \bar{L}^*, \Xi) \]

with \( \bar{L}^* = (V_{dc1}^*, V_{dc2}^*, P_{out}^*)^T \)

— Choose Control Parameters \( \Xi^* \) so as to Minimize Transformer RMS Current \( I_{ac1,\text{rms}} \)
Modulation Schemes

- 3-Level Dual Active Bridge
- 5-Level Dual Active Bridge

- Significantly Lower RMS Currents of 5L-DAB Due to Higher DOF of Modulation
Modulation Schemes - Zero Voltage Switching (1)

\[ W_{t1} = E_{\text{oss}}(V_{\text{dc}}) + \frac{1}{2} L_\sigma I_1^2 \]
Modulation Schemes - Zero Voltage Switching (2)

\[ W_{t1} = E_{oss}(V_{dc}) + \frac{1}{2} L_\sigma I_1^2 \]

\[ i_L(t_2) = 0 \]

\[ W_{t2} = E_{oss}(V_{dc}) + Q_{oss}(V_{dc}) \cdot V_{dc} \]
Modulation Schemes - Zero Voltage Switching (3)

\[ W_{t1} = E_{oss}(V_{dc}) + \frac{1}{2} L_\sigma I_1^2 \]

\[ W_{t2} = E_{oss}(V_{dc}) + Q_{oss}(V_{dc}) \cdot V_{dc} \]

\[ \frac{1}{2} L_\sigma I_1^2 \geq Q_{oss}(V_{dc}) \cdot V_{dc} \]
Modulation Schemes - Zero Voltage Switching (4)

- Achieving ZVS
  - $L_\sigma$ Usually Provides Not Enough Charge
  - Add $L_m$ for Additional (Reactive) Current
  - At Low Power and/or Too Short Dead Time Intervals Still not Sufficient $\rightarrow$ Partial ZVS / Add. Switching Losses

- 3-Level Dual Active Bridge

- 5-Level Dual Active Bridge
Components and Materials

Power Semiconductors

- Si IGBT
  - Inexpensive
  - 1200 V
  - Cond. Losses Not Scalable
  - No ZVS Possible
  - Tail Currents
  - ZCS Difficult to Achieve

- Si SJ MOSFET
  - Conduction Losses Scalable
  - ZVS But Non-Zero Sw. Losses (!)

- SiC VD-MOSFET
  - Cond. Losses Scalable
  - Very Low ZVS Losses
  - 1200 V
  - Low Specific $C_{oss}$
  - Costs

Si IGBT

Si SJ MOSFET

SiC VD-MOSFET

Power Semiconductors

Si IGBT

Si SJ MOSFET

SiC VD-MOSFET

Cond. Losses Scalable
ZVS But Non-Zero Sw. Losses (!)
Large Specific $C_{oss}$
Only 650 V
NPC Half-Bridge Necessary
Increased Part Count
Cond. Losses Scalable
Very Low ZVS Losses
1200 V
Low Specific $C_{oss}$
Costs
Overview of Components and Materials

- **3-Level Dual Active Bridge**
  - CREE SiC MOSFET 80 mΩ 1200 V
  - 2 x on Variable Voltage Side
  - 1 x on Fixed Voltage Side

- **5-Level Dual Active Bridge**
  - CREE SiC MOSFET 80 mΩ 1200 V
  - Scaled 600 V SiC Switch
  - Variable Chip Sizes
  - Same Total Semicond. Cost as 3L-DAB

  - Optimized Aluminum Heat Sinks
  - Range of Low Power DC Fans

  - EPCOS N87 Ferrite E & ELP Cores
  - Litz Wire with Range of Strand Diameters

  - EPCOS MKP DC Film Capacitors
  - 575 V and 1100 V Rated
Global Optimization Routine (1)

- Design Space
- Operating Points $\bar{A}_{\text{opt},a}$
- Constraints & Parameters
- Component Database

$J_{sw}$

$j = j + 1$

Global System Optimization

Dependent Global Design Variables

Calculate Dependent Global Design Variables:

- $T_{d,\text{max}} = 2.5\% \cdot T_{sw}$
- $\Delta V_{\text{pp, max}} = 2V$
- $\bar{A}_{\text{chip}} = \bar{A}_{\text{chip}}^*$

- $n = n^*$
- $L_a = L_a^* \cdot \frac{I_{sw}}{I_{sw}}$
- $L_m = L_m^* \cdot \frac{I_{sw}}{I_{sw}}$

$T_{d,\text{max},j}$, $L_a,j$, $L_m,j$, $\bar{C}_{G,j}$

Calculate WC and Nominal Waveforms

Waveforms

Global Optimization

Local Component Optimization

Identify & Store Pareto-Optimal Designs $D_{\text{sw},j}$

$j < j_{\text{tot}}$ Yes

No

Identify Overall $n_{\text{avg}}, \rho_{\text{max}}, \sigma_p$ Pareto-Optimal Designs $D_{\text{DAB}}$
Global Optimization Routine (2)

- Offline Design Variable Optimization

- $L_\sigma$, $L_m$, and $n$ Determine Waveforms
- Optimize with Chip Area Distribution

- Minimum Semiconductor Losses
- ZVS for All Operating Points
- Design Frequency: 50 kHz
Optimization Results - Pareto Surfaces (1)

- 3-Level Dual Active Bridge

![Graphs showing optimization results for 3-Level Dual Active Bridge](image_url)
Optimization Results - Pareto Surfaces (2)

5-Level Dual Active Bridge

- Average Efficiency $\eta_{\text{avg}}$ vs. Power Density $\rho_{\text{box}}$ (kW/dm$^3$)
- Average Efficiency $\eta_{\text{avg}}$ vs. Watts per Euro $\sigma_{p}$ (W/€)
- Watts per Euro $\sigma_{p}$ vs. Power Density $\rho_{\text{box}}$ (kW/dm$^3$)
- Watts per Euro $\sigma_{p}$ vs. Power Density $\rho_{\text{box}}$ (kW/dm$^3$) in 3D
Optimization Results - Component Breakdown (1)

- Lower RMS Currents Overcompensated by Low Chip Utilization
- Higher 5L-DAB Conduction Losses $P_c$
- Lower 5L-DAB Switching Losses $P_{sw}$ and Incomplete ZVS $P_{izVS}$ Losses
  Due to More Uniform Current Waveforms
Optimization Results - Component Breakdown (2)

- Higher 5L-DAB Volume Mainly Due to Higher Capacitance for Midpoint Balancing
- Increase of Magnetics Volume at High $f_{sw}$ Due to High Core Losses
- Auxiliary Based on Prototype – Industrial Auxiliary Approx. Half the Volume
- Higher $f_{sw}$ Allows for Lower Volume of Passives
- However, Magnetics Require More Expensive Litz Wire, Capacitors are Inexpensive
- Main Costs are Semiconductors and Auxiliary
- Auxiliary (incl. Gate Drivers) Based on Prototype – Industrial Auxiliary Approx. Half the Costs

**Optimization Results - Component Breakdown (3)**

![Graph showing cost breakdown for 8 vs. 12 Gate Driver Units]
Experimental Verification (1)

- Hardware Prototype of Three-Level Dual Active Bridge (3L-DAB)

\[ P = 5 \text{ kW} \]
\[ V_i = [100, 700] \text{ V} \]
\[ V_o = 750 \text{ V} \]
\[ f_{\text{SW}} = 50 \text{ kHz} \]
\[ V_{\text{box}} = 2.8 \text{ dm}^3 (171 \text{ in}^3) \]

- Power Density 1.8 kW/dm³
- Peak Efficiency 98.5%
- Average Efficiency 97.6%
Experimental Verification (2)

- Very High Efficiency Despite High Functionality

- Peak Efficiencies of 98.8% (Without Auxiliary) and 98.5% (incl. 10W Aux. Power)
- High Efficiency Over Extremely Wide Parameter Range
- ZVS in Most Operating Points
Experimental Verification (3)

- Very High Model Accuracy

- Average Error 2.5%
- Maximum Error 7.8%
- Widely Varying Mix of Loss Contributions
Experimental Verification (4)

- High Accuracy of Thermal Modeling

- Supports Calculated Loss Modeling
- Temperatures Generally Underestimated → Wiring, Thermal Coupling
Experimental Verification (5)

- Accuracy Prediction of Voltage and Current Waveforms

- Non-Linear Switching-Transitions
- Incomplete ZVS Transitions
Experimental Verification (6)

- Comparison to Pareto Surface

Prototype Development

* No Optimization Routine
* Target Power Density of 2.0 kW/dm³

Improvements with Advanced Multi-Objective Optimization

* 0.3% Higher Eff. @ Same Volume/Costs
* 40% Lower Volume and 20% Lower Costs @ Same Efficiency
Conclusions Example I

- **3L-DAB Clearly Superior over 5L-DAB**
  - More Efficient (Chip Area Utilization)
  - Higher Power Density (Capacitors)
  - Lower Costs (Gate Drivers)
  - Much Simpler → Reliability
  - High Functionality (Voltage Range, Galv. Isolation, Bidir.) @ High Efficiency
  - Could not be Achieved w/o SiC

- **ZVS**
  - Difficult to Achieve at Low Load and/or High Switching Frequencies
  - Parasitic Capacitances (Semicond. Package (!) to Heat Sink, Magnetics, PCB Layout) Become Highly Important Due to Required Add. Charge

- **Usefulness of Multi-Objective Optimization Routine**
  - High Accuracy of Models
  - Improvements for Prototype Revealed
Converter Optimization
Example II

DC/AC PV Application
Topologies/Modulation Schemes
Materials/Components
Optimization
Pareto Surfaces
LCC Post-Processing
Motivation (1)

- Advancements in PV Converter Design and Development
  - 1990s – 2000s
    * Main Focus on Efficiency
    * Improvements from 90% to >98%
  - 2010s
    * Econom. Downturn and Slower Market Growth
    * Main Focus on Costs (!)

- Ongoing Discussion on Whether and How SiC Can Improve PV-Inv. Performance (!)

1992 $\eta = 93\%$

2007 $\eta = 96\%$

2011 $\eta = 99\%$

Future?
Motivation (2)

Opportunities of SiC in PV Applications

1. Same Sw. Freq. and Higher Eff. at Same Volume → Costs?
2. Higher Sw. Freq. and Lower Volume at Same Eff. → Costs?
3. Other Topologies/Modul. Schemes (e.g. Higher Voltages, ZVS Operation, 2-Level, etc...)

Systematic Multi-Objective Optimization Imperative!

State of Research

- Only Very Few Contributions with Multi-Objective Optimization
- Mostly Case Studies of Single Prototype and Single Frequency, Main Inductance etc.

Optimal?

ETH zürich
Application and Goals

- Single-Input/Single-MPP-Tracker Multi-String PV Converter
- DC/DC Boost Converter for Wide MPP Voltage Range
- Output EMI Filter
- Typical Residential Application

Systematic Multi-Objective $\eta - \rho - \sigma$-Comparison of Si vs. SiC
- Exploit Excellent Hard- AND Soft-Switching Capabilities of SiC
- Find Useful Switching Frequency and Current Ripple Ranges
- Find Appropriate Core Material
**Topologies - Converter Stages**

- **All Si IGBT 3-Level PWM Inverter (3L-PWM)***

- **All SiC MOSFET 2-Level PWM Inverter (2L-PWM)***

- **All SiC MOSFET 2-Level Double-Interleaved TCM-Inverter (2L-TCM)***
Topologies - Filter Stages

- 2-Stage DM & CM Filter for 2L-PWM and 3LP-WM
- 2-Stage DM & CM Filter for 2L-TCM
- TCM Inductor Acting as DM & CM Inductance
Modulation Schemes - PWM Converters

■ Three-Level PWM Inverter (3L-PMW)
  — Symmetric Boost Converter
  — Interleaved Operation
  — Part. Compensation of LF DC-Link Midpoint Variation
  — 3-Level T-Type Converter
  — 3-Level PWM Modulation
  — 3rd Harmonic Injection

■ Two-Level PWM Inverter (2L-PMW)
  — Standard DC/DC Booster
  — Standard Modulation
  — 2-Level Converter
  — 2-Level PWM Modulation
  — 3rd Harmonic Injection
Modulation Schemes - TCM Converter

- Two-Level TCM Inverter (2L-TCM)
  - 2-Level/Double Interleaved Booster
  - Interleaved TCM Operation
  - Turn-Off of Branch in Partial Load
  - 2-Level/Double Interleaved Booster
  - Interleaved TCM Operation
  - Turn-Off of Branch in Partial Load

- ZVS for All Sw. Transitions
- Variable $f_{sw}$
- $I_{min}$ to Limit $f_{sw}$
- Losses Due to $I_{min}$ @ Low Loads
### Components and Materials

#### 3L-PWM
- 6 x Infineon Si IGBT H3 25 A 1200 V / PiN Diode
- 6 x Infineon Si IGBT T&F 30 A 600 V / PiN Diode
- 2 x Infineon Si IGBT T&F 30 A 600 V
- Infineon Si PiN Diode 45 A 600 V

#### 2L-PWM
- 7 x CREE SiC MOSFET 80 mΩ 1200 V
- 1 x CREE SiC Schottky Diode 20 A 1200 V

#### 2L-TCM
- 16 x CREE SiC MOSFET 80 mΩ 1200 V

#### Power Semiconductors
- Optimized Al Heat Sinks
- Range of Sanyo Low Power Long Life DC Fans

#### Cooling System
- METGLAS 2605SA1 Amorphous Iron C Cores
- Solid Round Wire
- EPCOS N87 Ferrite E Cores
- Litz Wire With Range of Strand Diameters

#### Main Induct.
- EPCOS MKP DC Film Capacitors 575V and 1100 V for MPP Cap.
- EPCOS Long Life Al Electrolytic Capacitors 500 V for DC-Link Cap.

#### DC Caps
- EPCOS X2 (DM/CM) and Y2 (CM) EMI Capacitors
- Magnetics KoolMu Gapless Powder Cores / Solid Round Wire (DM)
- VAČ Vitroperm 250F/500F Nanocrystalline Toroid Cores / Solid Round Wire (CM)
Global Optimization Routine

- **Independent Design Variables**
  - 3L-PWM
    \[ \tilde{f}_{3L\text{-PWM}}: f_{sw} \in [6, 36] \text{ kHz}, \quad \Delta I_{L,max}^{pp} \in [5, 60] \% \]
  - 2L-PWM
    \[ \tilde{f}_{2L\text{-PWM}}: f_{sw} \in [12, 72] \text{ kHz}, \quad \Delta I_{L,max}^{pp} \in [5, 60] \% \]
  - 2L-TCM
    \[ \tilde{f}_{2L\text{-TCM}}: f_{sw,\text{min}} \in [12, 84] \text{ kHz}, \quad k_{fsw} \in [4, 12] \]

- **Dependent Design Variables**
  - Main Inductances Function of \( f_{sw} \) and \( \Delta I_{L,max}^{pp} \)
  - Filter Components Based on CISPR Class B

- **European Efficiency**
  \[ \eta_{\text{euro}} = 0.05 \cdot \eta_{0.03-P_i} + 0.1 \cdot \eta_{0.1-P_i} + 0.2 \cdot \eta_{0.2-P_i} + 0.3 \cdot \eta_{0.3-P_i} + 0.5 \cdot \eta_{0.5-P_i} + 1 \cdot \eta_{1.0-P_i} \]
  - Add. Weighted for \{525, 575, 625\} V MPP Voltage
Optimization Results - Pareto Surfaces (1)

- No Pareto-Optimal Designs for $f_{\text{sw,min}} > 60$ kHz
- No METGLAS Amorphous Iron Designs
- Pareto-Optimal Designs for Entire Considered $f_{\text{sw}}$ Range
- No METGLAS Amorphous Iron Designs
- Pareto-Optimal Designs for Entire Considered $f_{\text{sw}}$ Range
- METGLAS Amorphous Iron and Ferrite Designs
Optimization Results - Pareto Surfaces (2)

- **3L-PWM Core Material**
  - Compact Designs with Amorphous Core Material @ Low Ripples
  - Cheap Designs with Ferrite @ High Ripples Despite Larger Volume

- **2L-TCM Core Material**
  - Only Ferrite for 2L-TCM Due Large HF Excitations
  - Expected Result

- **2L-PWM Core Material**
  - Ferrite @ High Ripples Cheaper AND Smaller - Unexpected Result (!)
  - Amorphous Core Material too High Losses Already @ Low Ripples, High Flux Density Not Exploited
Optimization Results – Component Breakdowns (1)

- Semiconductor Losses Clearly Dominating (35 to 70%)
Optimization Results – Component Breakdowns (2)

- DC Caps of 3L-PWM Largest Because of Midpoint Variation / Balancing
Higher Gate Driver Costs (incl. in Aux.) of 3L-PWM Compensates Lower Si Semicond. Costs
Optimization Results - Semiconductor Losses

- Sensitivities of Semiconductor Losses

- **2L-TCM**
  - Wide Sw. Frequency Range / Lower $I_{\text{min}}$ Results in Lower Conduction Losses

- **2L-PWM**
  - High Ripple Operation
  - Lower Switching Losses Due ZVS

- **3L-PWM**
  - No ZVS for IGBTs
  - High Ripples are Causing Higher Cond. Losses
Extension to Multi-Objective Optimization Approach

Performance Space Analysis

- 3 Performance Measures: $\eta$, $\rho$, $\sigma$
- Reveals Absolute Performance Limits / Trade-Offs Between Performances

LCC Analysis

- Post-Processing of Pareto-Optimal Designs
- Determination of Min.-LCC Design
- Arbitrary Cost Function Possible

Which is the Best Solution? Weighting $\eta$, $\rho$, $\sigma$, e.g. in Form of Life-Cycle Costs (LCC)?

How Much Better is the Best Design?

Optimal Switching Frequency?
Post-Processing

- LCC – Analysis (1)

Simple Life-Cycle Costs (LCC) Function for Mapping into 1D Cost Space
- Initial Costs, Capital Costs and Lost Revenue (=Losses) Based on Net-Present-Value (NPV) Analysis

\[
LCC = \Sigma_{\text{tot}} + \sum_{n=1}^{N} \left\{ q \cdot \Sigma_{\text{tot}} + \Sigma_{\text{losses}}(\eta_{\text{euro}}) \right\} \cdot \frac{1}{(1+q)^n}
\]

- Assumptions
  \[q = 5\% / \text{year} \quad N = 10 \text{ years}\]
**Post-Processing**

- **LCC – Analysis (2)**

- **Best System**
  - 2L-PWM @ 44kHz & 50% Ripple
    - 22% Lower LCC than 3L-PWM
    - 5% Lower LCC than 2L-TCM
    - Simplest Design
    - Probably Highest Reliability
    - Volume Advantage Not Considered Yet (Housing!)
Conclusions - Example II

- **SiC Systems Superior to State-of-The-Art Si System**
  - Generally Higher Efficiency and Power Density of SiC
  - Initial Costs only Marginally Lower (SiC 2L-PWM) or Higher (SiC 2L-TCM)
  - TCM Operated System More Complex but With Highest Potential for Further Improvements

- **LCC Analysis to Determine Optimal Design**
  - SiC 2L-PWM @ 44 kHz vs. Si 3L-PWM @ 18 kHz → 22% Lower LCC of SiC
  - Initial Costs 5% Lower
  - Smaller Housing and Higher Reliability Not Considered Yet

- **Usefulness of Multi-Objective Optimization Routine**
  - SiC can Improve $\eta$, $\rho$, and $\sigma$ Simultaneously
  - Optimal Switching Frequencies Lower than in Previous Publications
  - Results/Findings Not Possible with $\eta$-, $\rho$- or $\eta$-$\rho$-Optimizations or Single Prototypes
Conclusions
Overall Summary

- Only Full System Level $\eta$-$\rho$-$\sigma$-Optimization Reveals Full Adv. of SiC (!)
  * Adv. Cannot be Identified for 1:1 Replacement or only 1D-Optimization

- Rel. Low Optimum SiC Sw. Frequencies Calculated Compared to Literature
  * 44kHz for 2L-SiC Inverter vs. 18kHz for 3L-Si-IGBT Inverter
  * Frequently Incomplete Models Employed in Publications

- Advantages of SiC Concerning Efficiency, Power Density & Costs
  * Lower System Complexity (2L vs. 3L) / Higher Reliability
  * Saving in Passives Overcompensates Higher SiC Costs

- SiC Allows Massive $\eta$-$\rho$-Gain vs. 1200V Si for High-Frequ. DC/DC Converters
  * Design for Minim. Parasitic Cap. to Ensure ZVS @ Low Effort
  * Research on HF Magnetics / TCM ZVS Schemes / Packaging Mandatory

SiC →  — Higher Efficiency / Power Density @ Same Costs
         — Lower Complexity / Higher Reliability
         — Higher Functionality
Future Design Process

- Main Challenges: Modeling (EMI, etc.) & Transfer to Industry

- Reduces Time-to-Market
- More Application Specific Solutions (PCB, Power Module, and even Chips)
- Only Way to Understand Mutual Dependencies of Performances / Sensitivities (!)
- Simulate What Cannot Any More be Measured (High Integration Level)
Future Research
Future Challenges

- Consider Converters like “Integrated Circuits”
- Extend Analysis to Converter Clusters / Power Supply Chains / etc.

- “Converter” → “Systems” (Microgrid) or “Hybrid Systems” (Autom. / Aircraft)
- “Time” → “Integral over Time”
- “Power” → “Energy”

\[ p(t) \to \int_{0}^{t} p(t) \, dt \]

- Power Conversion → Energy Management / Distribution
- Converter Analysis → System Analysis (incl. Interactions Conv. / Conv. or Load or Mains)
- Converter Stability → System Stability (Autonom. Cntrl of Distributed Converters)
- Cap. Filtering → Energy Storage & Demand Side Management
- Costs / Efficiency → Life Cycle Costs / Mission Efficiency / Supply Chain Efficiency
- etc.
New Power Electronics Systems Performance Figures/Trends

Complete Set of New Performance Indices

- Power Density \([\text{kW/m}^2]\)
- Environmental Impact \([\text{kWs/kW]}\)
- TCO \([\$/\text{kW]}\)
- Mission Efficiency \([\%]\)
- Failure Rate \([\text{h}^{-1}]\)
References


About the Speakers

**Johann W. Kolar** is a Fellow of the IEEE and is currently a Full Professor and the Head of the Power Electronic Systems Laboratory at the Swiss Federal Institute of Technology (ETH) Zurich. He has proposed numerous novel PWM converter topologies, and modulation and control concepts and has supervised over 50 Ph.D. students. He has published over 650 scientific papers in international journals and conference proceedings and 3 book chapters, and has filed more than 120 patents. He received 21 IEEE Transactions and Conference Prize Paper Awards, the 2014 IEEE Middlebrook Award, and the ETH Zurich Golden Owl Award for excellence in teaching. The focus of his current research is on ultra-compact and ultra-efficient SiC and GaN converter systems, wireless power transfer, Solid-State Transformers, Power Supplies on Chip, and ultra-high speed and bearingless motors.

**Ralph M. Burkart** received his M.Sc. degree in electrical engineering from the Federal Institute of Technology (ETH), Zurich, Switzerland, in 2011. During his studies, he majored in power electronics, electrical machines and control engineering. In the framework of his Master Thesis he designed and implemented a high-dynamic inverter system for active magnetic bearings in an ultra-high speed electrical drive system. Since 2011, he has been a Ph.D. student at the Power Electronic Systems Laboratory at ETH Zurich. His main research area is multi-domain modeling of power electronics components and multi-objective optimization of photovoltaic DC/DC and DC/AC converter systems employing SiC power semiconductors.
Thank You!
Questions