Three-Phase PFC Rectifier and AC-AC Converter Systems

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Outline

- Introduction to Three-Phase PFC Rectifier Systems
- Passive and Hybrid Rectifier Systems

Coffee Break

- Unidir. Phase-Modular PFC Rectifier Systems
- Unidir. Boost-Type Two- and Three-Level Active PFC Rectifier Systems

Coffee Break

- Unidir. Buck-Type PFC Rectifier Systems
- Summary of Unidir. Rectifier Systems

Coffee Break

- Bidirectional PFC Rectifier Systems
- Extension to AC/DC/AC and AC/AC Converter Systems
- Conclusions / Questions / Discussion

- Multi-Domain Simulator Based Design (GECKO)
Part 1
Three-Phase PFC Rectifier Systems
Outline

Unidirectional Rectifier Systems
► Passive Systems
► Hybrid Systems
► Active PFC Systems
► Comparative Evaluation

Bidirectional Rectifier Systems
► Two-Level Converters
► Three-Level Converters
Classification of Unidirectional Rectifier Systems

Unidirectional Three-Phase Rectifier Systems

- Passive Systems
  - Single Diode Bridge
    - DC-Side Inductor
    - AC-Side Inductors
    - Passive 3rd Harmonic Injection
  - Multi-Pulse Rect. System
    - (Partial) Transf. Isol. or Auto-Transf.-Based
    - AC- or DC-Side Interph. Transformer
    - Passive Pulse Multiplication

- Hybrid Systems
  - Electronic Reactance Based
    - Single Diode Bridge & DC-Side Electron. Ind.
    - Single Diode Bridge & AC-Side Electron. Ind. or Cap.
    - Multi-Pulse Rectifier System Employing Electron. Inter-phase Transf.
  - Combination of Diode Rectifier and DC/DC Converter
    - Boost-Type
      - Single Diode Bridge & DC/DC Output Stage
      - Half-Controlled Diode Bridge
      - Multi-Pulse Rect. System (Transf. or Auto-Transf.-Based)
      - DC/DC Output Stage Empl. AC-Side or DC-Side Ind.
    - Buck-Type
      - Single Diode Bridge & DC/DC Output Stage
      - Half-Controlled Diode Bridge
  - Active 3rd Harmonic Injection
    - Passive/Hybrid or Active 3rd Harm. Inject. Network
    - Boost- or Buck-Type or Uncontrolled Output
    - Diode Bridge or Multipulse System With Harmonic Inj. (Pulse Multipl.)

- Active PFC Systems
  - Direct Three-Phase Systems
    - Impressed Input Current (Boost-Type)
      - DCM
      - Single-Switch
      - Two-Switch
  - Pressed Input Voltage (Buck-Type)
    - CCM
    - Two-Level Converter
      - Y-Switch
      - Δ-Switch
      - Y-Arrangement With Mains Artificial Star-Point Connection
      - Three-Level Converter (VIENNA Rectifier)
    - DVM
      - Single-Switch Converter
    - CVM
      - Three-Switch Converter
      - Six-Switch Converter
  - Phase-Modular Systems
    - Y-Rectifier
    - Delta-Rectifier
    - 3/2-Phase Scott-Transf. Based
Classification of Unidirectional Rectifier Systems

Definitions and Characteristics

- **Passive Rectifier Systems**
  - Line Commutated Diode Bridge/Thyristor Bridge - Full/Half Controlled
  - Low Frequency Output Capacitor for DC Voltage Smoothing
  - Only Low Frequency Passive Components Employed for Current Shaping, No Active Current Control
  - No Active Output Voltage Control

- **Hybrid Rectifier Systems**
  - Low Frequency and Switching Frequency Passive Components and/or
  - Mains Commutation (Diode/Thyristor Bridge - Full/Half Controlled) and/or Forced Commutation
  - Partly Only Current Shaping/Control and/or Only Output Voltage Control
  - Partly Featuring Purely Sinusoidal Mains Current

- **Active Rectifier Systems**
  - Controlled Output Voltage
  - Controlled (Sinusoidal) Input Current
  - Only Forced Commutations / Switching Frequ. Passive Components

- **Phase-Modular Systems**
  - Phase Rectifier Modules of Identical Structure
  - Phase Modules connected in Star or in Delta
  - Formation of Three Independent Controlled DC Output Voltages

- **Direct Three-Phase Syst.**
  - Only One Common Output Voltage for All Phases
  - Symmetrical Structure of the Phase Legs
  - Phase (and/or Bridge-)Legs Connected either in Star or Delta
Classification of Unidirectional Rectifier Systems

Unidirectional Three-Phase Rectifier Systems

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  - AC-Side Inductors
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- Multi-Pulse Rect. System
  - (Partial) Transf. Isol. or Auto-Transf.-Based
  - AC- or DC-Side Interph. Transformer
  - Passive Pulse Multiplication

Hybrid Systems
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  - Single Diode Bridge & DC-Side Electron. Ind.
  - Single Diode Bridge & AC-Side Electron. Ind. or Cap.
  - Multi-Pulse Rectifier System Employing Electron. Inter-phase Transf.
- Combination of Diode Rectifier and DC/DC Converter
  - Boost-Type
    - Single Diode Bridge & DC/DC Output Stage
    - Half-Controlled Diode Bridge
    - Multi-Pulse Rect. System (Transf. or Auto-Transf.-Based) with DC/DC Output Stage Empl.
      AC-Side or DC-Side Ind.
  - Buck-Type
    - Single Diode Bridge & DC/DC Output Stage
    - Half-Controlled Diode Bridge

Active 3rd Harmonic Injection
- Passive/Hybr. or Active 3rd Harm. Inject. Network
- Boost- or Buck-Type or Uncontrolled Output
- Diode Bridge or Multipulse System With Harmonic Inj. (Pulse Multipl.)

Active PFC Systems
- Direct Three-Phase Systems
  - Impressed Input Current (Boost-Type)
    - DCM
    - Single-Switch
    - Two-Switch
  - CCM
    - Two-Level Converter
      - Y-Switch
      - Δ-Switch
      - Y-Arrangement With Mains Artificial Star-Point Connection
    - Three-Level Converter (VIENNA Rectifier)
- Impressed Input Voltage (Buck-Type)
  - DVM
  - CVM
    - Three-Switch Converter
    - Six-Switch Converter
Diode Bridge Rectifier with Capacitive Smoothing

\( U_{LL} = 3 \times 400 \) V
\( f_N = 50 \) Hz
\( P_{out} = 2.5 \) kW \((R=125 \ \Omega)\)
\( C = 1 \) mF; 40 µF
\( X_c/R = 0.025; 0.636 \)
Diode Bridge Rectifier / DC-Side Inductor and Output Capacitor

\[ U_{LL} = 3 \times 400 \, \text{V} \]
\[ f_N = 50 \, \text{Hz} \]
\[ P_{out} = 2.5 \, \text{kW} \quad (R=125 \, \Omega) \]
\[ C = 1 \, \text{mF} \]
\[ L = 5 \, \text{mH}; 20 \, \text{mH} \]
Diode Bridge Rectifier / AC-Side Inductor and Output Capacitor

\[ U_{LL} = 3 \times 400 \text{ V} \]
\[ f_N = 50 \text{ Hz} \]
\[ P_{out} = 2.5 \text{ kW} \ (R=125 \ \Omega) \]
\[ C = 1 \text{ mF} \]
\[ L = 2 \text{ mH}; 20 \text{ mH} \]
Passive 3\textsuperscript{rd} Harmonic Injection

\[
3f_N = \frac{1}{2\pi \sqrt{L_s C_s}} = \frac{1}{2\pi \sqrt{L_p C_p}}
\]

\[
R \approx \frac{1}{I}
\]

\[
\frac{u_1 + u_2}{2}
\]
- **Passive 3\(^{rd}\) Harmonic Injection**

- *Minimum THD of Phase Current for* \(i_y = \frac{1}{2} I\)
- \(\text{THD}_{\text{min}} = 5\%\)
Classification of Unidirectional Rectifier Systems

Unidirectional Three-Phase Rectifier Systems

- Passive Systems
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    - Passive 3rd Harmonic Injection
  - Multi-Pulse Rect. System
    - (Partial) Transf. Isol. or Auto-Transform.-Based
    - AC- or DC-Side Interph. Transformer
    - Passive Pulse Multiplication

- Hybrid Systems
  - Active 3rd Harmonic Injection
    - Passive/Hybrid or Active 3rd Harm. Inject. Network
    - Boost- or Buck-Type or Uncontrolled Output
    - Diode Bridge or Multipulse System With Harmonic Inj. (Pulse Multipl.)

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    - Impressed Input Current (Boost-Type)
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      - Two-Level Converter Y-Switch
      - Δ-Switch
      - Y-Arrangement With Mains Artificial Star-Point Connection
      - Three-Level Converter (VIENNA Rectifier)
  - Phase-Modular Systems
    - Impressed Input Voltage (Buck-Type)
      - DVM
        - Single-Switch Converter
      - CVM
        - Three-Switch Converter
      - Six-Switch Converter
      - Y-Rectifier
      - Delta-Rectifier
      - 3/2-Phase Scott-Transf. Based
Auto-Transformer-Based-12-Pulse Rectifier Systems

- AC-Side Interphase Transf. (Impr. DC Voltage)

- DC-Side Interphase Transf. (Impr. DC Current)

DC-Side Interphase Transformer can be omitted in Case of Full Transformer Isolation of Both Diode Bridges
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  - Combination of Diode Rectifier and DC/DC Converter
    - Boost-Type
      - Single Diode Bridge & DC/DC Output Stage
      - Half-Controlled Diode Bridge
      - Multi-Pulse Rect. System (Transf. or Auto-Transf.-Based) with DC/DC Output Stage Empl. AC-Side or DC-Side Ind.
    - Buck-Type
      - Single Diode Bridge & DC/DC Output Stage
      - Half-Controlled Diode Bridge

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  - Boost- or Buck-Type or Uncontrolled Output
  - Diode Bridge or Multipulse System With Harmonic Inj. (Pulse Multipl.)

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  - Direct Three-Phase Systems
    - Impressed Input Current (Boost-Type)
      - DCM
      - Single-Switch
      - Two-Switch
    - CCM
      - Two-Level Converter
        - Y-Switch
        - A-Switch
        - Y-Arrangement With Mains Artificial Star-Point Connection
        - Three-Level Converter (VIENNA Rectifier)
  - Phase-Modular Systems
    - Impressed Input Voltage (Buck-Type)
      - DVM
      - Single-Switch Converter
      - Three-Switch Converter
      - Six-Switch Converter
      - 3/2-Phase Scott-Transf. Based

- Y-Rectifier
- Delta-Rectifier
Diode Bridge and DC-Side Electronic Inductor (EI)

+ Only Fract. of Output Power Processed
+ High Efficiency and Power Density

– Not Output Voltage Control
– EMI Filtering Required
Diode Bridge and DC-Side Electronic Inductor (EI)

Control Structure

- Current Control could Theoretically Emulate Infinite Inductance Value but Damping (Parallel Ohmic Component) has to be Provided for Preventing Oscillations
Diode Bridge and DC-Side Electronic Inductor (EI)

Experimental Results

\[ U_{LL} = 3 \times 400 \, V \]
\[ P_o = 5 \, kW \]
\[ f_s = 70 \, kHz \]
\[ C = 4 \times 330 \, \mu F / 100 \, V \]

\[ \eta = 98.3 \% \]
\[ \lambda = 0.955 \]
\[ THD = 28.4 \% \]
Diode Bridge and DC-Side EI or Electronic Capacitor

- MERS Concept (Magnetic Energy Recovery Switch)

**Fundamental Frequency Equivalent Circuit**

![Diode Bridge and DC-Side EI or Electronic Capacitor Diagram]
12-Pulse Rectifier Employing Electr. Interphase Transformer (EIT)

- Switching Frequency DC-Side Inductors
- Proper Control of the EIT Allows to Achieve Purely Sinusoidal Mains Current!
Classification of Unidirectional Rectifier Systems

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Active 3rd Harmonic Injection
- Passive/Hybrid or Active 3rd Harm. Inject. Network
- Boost- or Buck-Type or Uncontrolled Output
- Diode Bridge or Multipulse System With Harmonic Inv. (Pulse Multipl.)

Electronic Reactance Based
- Single Diode Bridge & DC-Side Electron. Ind.
- Single Diode Bridge & AC-Side Electron. Ind. or Cap.

Boost-Type
- Single Diode Bridge & DC/DC Output Stage
- Half-Controlled Diode Bridge
- Multi-Pulse Rect. System (Transf. or Auto-Transf.-Based) with DC/DC Output Stage Empl. AC-Side or DC-Side Ind.

Buck-Type
- Single Diode Bridge & DC/DC Output Stage
- Half-Controlled Diode Bridge

Hybrid Systems

Impressed Input Current (Boost-Type)
- Single-Switch
- Two-Switch
- DCM
- Two-Level Converter
- Y-Switch
- A-Switch
- Y-Arrangement With Mains Artificial Star-Point Connection
- Three-Level Converter (VIENNA Rectifier)

Impressed Input Voltage (Buck-Type)
- Single-Switch Converter
- DVM
- CVM
- Three-Switch Converter
- Six-Switch Converter

Active PFC Systems

Phase-Modular Systems
- Y-Rectifier
- Delta-Rectifier
- 3/2-Phase Scott-Transf. Based
Active 3rd Harmonic Injection into All Phases

- No Output Voltage Control
- Mains Current Close to Sinusoidal Shape

![Diagram](image)

- Controlled Output Voltage
- Purely Sinusoidal Shape of Mains Current

\[ i_1 = I + \frac{3}{2} i_y \]
\[ i_2 = I - \frac{3}{2} i_y \]

CCL: \[ 3i_y = i_1 - i_2 \]

Minnesota Rectifier
Active 3\textsuperscript{rd} Harmonic Injection into All Phases

\[ \omega t \in \left[ 0, \frac{\pi}{3} \right] \]

\[ i_a = \hat{I} \cos(\omega t) \]
\[ i_b = \hat{I} \cos\left(\omega t - \frac{2\pi}{3}\right) \]
\[ i_c = \hat{I} \cos\left(\omega t + \frac{2\pi}{3}\right) \]

\[ i_y = -i_b \]
\[ i_1 = i_a + i_y \]
\[ i_2 = -(i_c + i_y) \]

\[ i_a + i_b + i_c = 0 \]
\[ i_1 - i_2 = i_a + i_y + i_c + i_y = -i_b + 2i_y = 3i_y \]

- Current Control Implementation with Boost-Type DC/DC Converter (Minnesota Rectifier) or with Buck-Type Topology
Active 3\textsuperscript{rd} Harmonic Inj. Only into One Phase (I)

- Purely Sinusoidal Mains Current (Only for Const. Power Load)
- Low Current Stress on Active Semicond. / High Efficiency
- Low Complexity

- No Output Voltage Control

\[ \omega t \in \left[ 0, \frac{\pi}{3} \right] \]

\[ \begin{align*}
T_+ & \quad T_- \\
0 & \quad 2
\end{align*} \]

\[ (1-k)i_y \]

\[ (1-k)i_y \]

\[ T_+ \quad T_- \]

Could be Replaced by Passive Network
- Current to be Inj. Into Phase $b$: \[ i_y = -i_b \]

- Local Avg. Ind. Voltage / Bridge Leg $(T_+, T_-)$ Output Voltage:
  \[ \bar{u}_L \approx 0 \quad \text{and/or} \quad \bar{u}_{20} = u_{b0} \]

- Bridge Leg Voltage Formation:
  \[ u_{b0} = k \cdot u_{ac} + u_{c0} \]
  \[ k = \frac{u_{bc}}{u_{ac}} \]

- Bridge Leg Current Formation:
  \[ \bar{i}_{T_+} = k \cdot i_y = -k \cdot G \cdot u_{b0} = -G \cdot u_{b0} \frac{u_{bc}}{u_{ac}} \]

- Constant Power Load Current:
  \[
  i = \frac{P}{u_{ac}} = \frac{u_{ac} \cdot i_a + u_{bc} \cdot i_b}{u_{ac}} = G \left( u_{a0} + u_{b0} \frac{u_{bc}}{u_{ac}} \right)
  \]

- Sinusoidal Mains Current:
  \[ i + \bar{i}_{T_+} = G \cdot u_{a0} = i_a \]
Active 3\textsuperscript{rd} Harmonic Inj. Only into One Phase (II)

- Boost-Type Topology
  + Controlled Output Voltage
  + Purely Sinusoidal Mains Current
  - Power Semiconductors Stressed with Line-to-Line and/or Full Output Voltage

- Proof of Sinusoidal Mains Current Shape for $\omega t = \left[0, \frac{\pi}{3}\right]$ (1)

- 4 Different Switching States:
  \[ \begin{align*}
  & T_+ \text{ on, } T_- \text{ off } \quad \{ k_1 \\
  & T_+ \text{ off, } T_- \text{ on } \quad \{ k_2 \\
  & T_+ \text{ off, } T_- \text{ off } \quad \{ k_3 = (1 - k_1 - k_2) \\
  & T_+ \text{ on, } T_- \text{ on } \quad \{ k_3 
  \end{align*} \]

3 Different States Regarding the Current Paths with Relative On-Times $k_1$, $k_2$, and $k_3$
Proof of Sinusoidal Mains Current Shape for $\omega \in \left[0, \frac{\pi}{3}\right]$ (2)

- **Current to be Injected into $b$:**
  \[ i^*_y = -i^*_b \]

- **Inductor Voltages:**
  \[ \overline{u}^*_{L,1} \approx 0 \quad \overline{u}^*_{L,2} \approx 0 \]

- **Bridge Leg ($T_+, T_-$): Voltage Form.:**
  \[ k_1 u_{ab} + k_2 \left( u_{ab} - U_{pn} \right) + (1 - k_1 - k_2) u_{ab} = 0 \]
  \[ k_2 = \frac{u_{ab}}{U_{pn}} \]
  \[ k_1 \left( u_{bc} - U_{pn} \right) + k_2 u_{bc} + (1 - k_1 - k_2) u_{bc} = 0 \]
  \[ k_1 = \frac{u_{bc}}{U_{pn}} \]

- **Constant Power, Load Current:**
  \[ \overline{i} = \frac{P}{U_{pn}} = \frac{u_{ab} i_a - u_{bc} i_c}{U_{pn}} = -k_1 i_c + k_2 i_a \]

- **Current Formation in $T_+$:**
  \[ \overline{i}_{T+} = k_1 i^*_y + (1 - k_1 - k_2) i^*_a \]
  \[ \text{Condition: } i^*_a + i^*_b + i^*_c = 0 \]

**Sinusoidal Mains Current:**
\[ \overline{i}_{T+} + \overline{i}^* = i^*_a \]
Active 3\textsuperscript{rd} Harmonic Inj. Only into One Phase (III)

- Buck-Type Topology
  - Controlled Output Voltage
  - Purely Sinusoidal Mains Current
  - Low Control Complexity

- Higher Number of Active Power Semiconductors than Active Buck-Type PWM Rect. (but Only $T_+\ D_+$ Operated with Switching Frequency)

- Patent Pending
- Switches Distributing the Injected Current could be Replaced by Passive Network

$U_{N,LL} = 400V_{\text{rms}}$
$U_{pn} = 400V_{\text{DC}}$
P=10kW
Proof of Sinusoidal Mains Current Shape for $\omega t \in \left[0, \frac{\pi}{3}\right]$

- Current to be Inj. into Phase $b$: $i_y = -i_b$

- Current Formation:
  
  \[ k_1 I = i_a \quad k_2 I = -i_c \]
  
  \[ i_y = -(1-k_1)I + (1-k_2)I = -i_b \]

\[ i_a + i_b + i_c = 0 \]

Duty Cycles:

\[ T_+ \rightarrow k_1 \]

\[ T_- \rightarrow k_2 \]

\[ i_a = G \cdot u_{a0} \]

\[ i_b = G \cdot u_{b0} \]

\[ i_c = G \cdot u_{c0} \]

- Local Avg. Ind. Voltage:
  
  $\bar{u}_L \approx 0$

- Voltage Formation:
  
  $k_1u_a + (1-k_1)u_b - (k_2u_c + (1-k_2)u_b) = u_{pn}$

  \[ k_1u_{ab} - k_2u_{cb} = u_{pn} \]

  \[ i_a u_{ab} + i_c u_{cb} = u_{pn} I \]

\[ i_a u_{ab} + i_c u_{cb} = P = \text{const.} \quad I = \text{const.} \rightarrow u_{pn} = \text{const.} \]
Classification of Unidirectional Rectifier Systems

Unidirectional Three-Phase Rectifier Systems

- Passive Systems
  - Single Diode Bridge & DC-Side Electron. Ind.
  - Multi-Pulse Rect. System
    - Passive 3rd Harmonic Injection

- Hybrid Systems
  - Passive System: (Partial) Transf. Isol. or Auto-Transf.-Based
  - Hybrid System: AC- or DC-Side Interph. Transformer
  - Hybrid System: Passive Pulse Multiplication

- Active PFC Systems
  - Hybrid System: Y-Rectifier
  - Hybrid System: Delta-Rectifier
  - Hybrid System: 3/2-Phase Scott-Transf. Based

Active 3rd Harmonic Injection

- Electronic Reactance Based
  - Single Diode Bridge & DC-Side Electron. Ind.
  - Single Diode Bridge & AC-Side Electron. Ind. or Cap.

- Combination of Diode Rectifier and DC/DC Converter
  - Boost-Type
    - Single Diode Bridge & DC/DC Output Stage
    - Half-Controlled Diode Bridge
    - Multi-Pulse Rect. System (Transf. or Auto-Transf.-Based) with DC/DC Output Stage Empl. AC-Side or DC-Side Ind.
  - Buck-Type
    - Single Diode Bridge & DC/DC Output Stage
    - Half-Controlled Diode Bridge

Impressed Input Current (Boost-Type)

- DCM
- CCM
- Two-Level Converter
- Single-Switch Converter
- Three-Level Converter

Impressed Input Voltage (Buck-Type)

- DVM
- CVM
- Three-Switch Converter
- Six-Switch Converter
Diode Bridge Combined with DC/DC Boost Converter

\[ U_{LL} = 3 \times 400 \text{ V} \ (f_N = 50 \text{ Hz}) \]
\[ P_{out} = 10 \text{ kW} \]
\[ \lambda = 0.952 \]
\[ \text{THD} = 32\% \]

Other Diode Bridge Output Current Impressing DC/DC Converter Topologies (e.g. SEPIC, Cuk) result in Same Mains Current Shape
Half-Controlled Rectifier Bridge Boost Converter

- Sinusoidal Current Control Only in Sectors with 2 Positive Phase Voltages, e.g. in Sector B
- In other Sectors, Only One Phase Current could be Shaped, e.g. in Sector A

+ Controlled Output Voltage \( (U > \sqrt{6} \hat{U}) \)
+ Low Complexity (e.g. Single Curr. Sensor)
+ Low Conduction Losses

- Block Shaped Mains Current
### Half-Controlled Rectifier Bridge Boost-Type Converter

#### Current Control Concepts

**Option 1:** All Switches Simultaneously Controlled with Same Duty-Cycle (Synchr. Modulation)

**Option 2:** Only Phase with most Positive Voltage is Modulated, Switch of Phase with most Neg. Voltage is Cont. Turned on for Lowering Conduction Losses in Case of Switch Implementation with MOSFETs. Middle Phase Switch is OFF; Results in Block Shaped Mains Current

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![Control Acc. to Option 2](image-url)
Boost-Type Auto-Transf.-Based 12-Pulse Hybrid Rectifier

- Impressed Diode Bridge Output Voltages

+ Output Voltage Controlled
+ Sinusoidal Mains Current Shaping Possible
- Active Converter Stage Processes Full Output Power
- Low Frequency Magnetics Employed
Boost-Type Auto-Transf.-Based 12-Pulse Hybrid Rectifier

Experimental Results (Impressed Diode Bridge Output Voltages)

\[ U_{LL} = 3 \times 115 \text{ V} \ (400 \text{ Hz}) \]
\[ P_0 = 10 \text{ kW} \]
\[ U_o = 520 \text{ V} \]
\[ f_s = 60 \text{ kHz} \]
\[ \text{THD}_i = 3.1\% \]
Boost-Type Auto-Transf.-Based 12-Pulse Hybrid Rectifier

- Impressed Diode Bridge Output Currents

  + Output Voltage Controlled
  + Sinusoidal Mains Current Shaping Possible

  - Active Converter Stage Processes Full Output Power
  - Low Frequency Magnetics Employed

Wide Varity of Further Topologies for Pulse Multiplication (e.g. 12p → 36p) which Process Only Part of Output Power but don’t Provide Output Voltage Control
Classification of Unidirectional Rectifier Systems

Unidirectional Three-Phase Rectifier Systems

- Passive Systems
  - Single Diode Bridge
  - Multi-Pulse Rect. System
- Hybrid Systems
  - (Partial) Transf. Isol. or Auto-Transf.-Based
  - AC- or DC-Side Interph. Transformer
  - Passive Pulse Multiplication

Electronic Reactance Based
- Combination of Diode Rectifier and DC/DC Converter
- Boost-Type
  - Single Diode Bridge & DC/DC Output Stage
  - Half-Controlled Diode Bridge
  - Multi-Pulse Rect. System (Transf. or Auto-Transf.-Based) with DC/DC Output Stage Empl. AC-Side or DC-Side Ind.
- Buck-Type
  - Single Diode Bridge & DC/DC Output Stage
  - Half-Controlled Diode Bridge

Active 3rd Harmonic Injection
- Passive/Hybrid or Active 3rd Harm. Inject. Network
- Boost- or Buck-Type or Uncontrolled Output
- Diode Bridge or Multipulse System With Harmonic Inj. (Pulse Multipl.)

Active PFC Systems
- Direct Three-Phase Systems
- Phase-Modular Systems
- Boost-Type
  - Single-Switch
  - Two-Switch
- Y-Switch
- ∆-Switch
- Y-Arrangement With Mains
- Artificial Star-Point Connection
- Three-Level Converter (VIENNA Rectifier)
- Buck-Type
  - Single-Switch Converter
  - Three-Switch Converter
  - Six-Switch Converter

- Y-Rectifier
- Delta-Rectifier
- 3/2-Phase Scott-Transf. Based
**Half-Controlled Rectifier Bridge Buck-Type Converter**

- **Controlled Output Voltage**
- **Low Complexity**
- **Low Conduction Losses**

- **Topology Limits Input Current Shaping to Intervals with Positive Phase Voltage**
  - **Sector 1:** Only $i_a$ could be Controlled
  - **Sector 2:** $i_a$ and $i_b$ could be Controlled

- **Low Complexity Control:** Only Current of Phase with most Positive Voltage Controlled; Switch of Phase with most Neg. Voltage Turned On Cont. for Providing a Free-Wheeling Path
Coffee Break!
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    - Passive 3rd Harmonic Injection
  - Multi-Pulse Rect. System
    - (Partial) Transf. Isol. or Auto-Transf.-Based
    - AC- or DC-Side Interph. Transformer
    - Passive Pulse Multiplication

- Hybrid Systems
  - Passive 3rd Harmonic Injection
    - Passive/Hybrid or Active 3rd Harm. Inject. Network
    - Boost- or Buck-Type or Uncontrolled Output
    - Diode Bridge or Multipulse System With Harmonic Inj. (Pulse Multipl.)

- Active PFC Systems
  - Direct Three-Phase Systems
    - Impressed Input Current (Boost-Type)
      - Single-Switch Converter
      - Two-Level Converter
        - Y-Switch
        - Δ-Switch
        - Y-Arrangement With Mains
        - Artificial Star-Point Connection
        - Three-Level Converter (VIENNA Rectifier)
    - CCM
    - DCM
  - Phase-Modular Systems
    - Impressed Input Voltage (Buck-Type)
      - Single-Switch Converter
    - Y-Rectifier
    - Delta-Rectifier
    - 3/2-Phase Scott-Transf. Based

Electronic Reactance Based

Combination of Diode Rectifier and DC/DC Converter

Boost-Type

- Single Diode Bridge
  & DC/DC Output Stage
- Half-Controlled Diode Bridge
- Multi-Pulse Rect. System
  (Transf. or Auto-Transf.-Based)
  with DC/DC Output Stage Empl.
  AC-Side or DC-Side Ind.

Buck-Type

- Single Diode Bridge
  & DC/DC Output Stage
- Half-Controlled Diode Bridge
- Multi-Pulse Rect. System
Phase-Modular Rectifier Topologies

- Y-Rectifier

- Δ-Rectifier

- Individual DC Output Voltages of the Phase Units
- Isolated DC/DC Converter Stages Required for Forming Single DC Output
Y-Rectifier

- Basic AC-Side Behavior Analogous to Direct Three-Phase Three-Level Rectifier Systems
**Y-Rectifier**

- Cond. States for $i_a > 0$, $i_b < 0$, $i_c < 0$ in Dep. on Transistor Switching States ($S_a S_b S_c$)

Switching States (011) and (100)

- Redundant Concerning Formation of $u_{ab}$, $u_{bc}$, $u_{ca}$
- Inverse Concerning Charging of $C_a$ and $C_c$ (and $C_b$)
Y-Rectifier

Equivalent Circuit and Voltage Formation

\[
\begin{align*}
    u_{\bar{a}} &= \bar{u}_{\bar{a}} + u_{\bar{a},}\sim \\
    u_{\bar{b}} &= \bar{u}_{\bar{b}} + u_{\bar{b},}\sim \\
    u_{\bar{c}} &= \bar{u}_{\bar{c}} + u_{\bar{c},}\sim \\
    u_{\bar{a}} &= u'_{\bar{a}} + u_0 \\
    u_{\bar{b}} &= u'_{\bar{b}} + u_0 \\
    u_{\bar{c}} &= u'_{\bar{c}} + u_0 \\
    u_0 &= \frac{1}{3} (u_{\bar{a}} + u_{\bar{b}} + u_{\bar{c}}) \\
    \bar{u}_{\bar{a}} &= \bar{u}'_{\bar{a}} + u_0 \\
    u_{\bar{a},}\sim &= u'_{\bar{a},}\sim + u_{0,}\sim
\end{align*}
\]

(Shown at the Example of Phase a)
Y-Rectifier

- Equivalent Circuit and Voltage Formation

\[ u_a + u_b + u_c = 0 \]

\[ u_a = L \frac{di_a}{dt} + \overline{u}_{a} + u'_{a,~} + u_{N''} \]

\[ u_b = L \frac{di_b}{dt} + \overline{u}_{b} + u'_{b,~} + u_{N''} \]

\[ u_c = L \frac{di_c}{dt} + \overline{u}_{c} + u'_{c,~} + u_{N''} \]

\[ 0 = 0 + 0 + 0 + 3u_{N''} \]

\[ u_{N''} = 0 \]

- Voltage of the Star Point \( N' \) Defined by \( u_0 \) (CM-Voltage)
Y-Rectifier

Modulation and Voltage Formation

- Addition of $m_0$ Increases Modulation Range from $\hat{U}_a = U$ to $\hat{U}_a = \frac{2}{\sqrt{3}}U$
- Potential of Star Point $N'$ Changes with LF ($\bar{u}_0$) and Switching Frequency ($u_{0,\sim}$)
**Y-Rectifier**

- Balancing of Phase-Module DC-Output Voltages by DC Component of $u_0$ ($\bar{m}_0$)

- $\bar{m}_0$ Only Changes the On-Time of Redundant Switching Stages, e.g. (100) and (011)

- No Influence on the AC-Side Current Formation—Allows Balancing of the Module Output Voltages Independent of Input Current Shaping
Y-Rectifier

- Control Structure / 2-out-of-3 Output Voltage Balancing

E.g.: \( \omega t \in \left[ 0, \frac{\pi}{3} \right] \)
- \( \max(u_a, u_b, u_c) = u_a \)
- \( \min(u_a, u_b, u_c) = u_c \)

- Output Voltage Balancing Considers Only Output Cap. Voltage of Phase with Max. Voltage (e.g. Phase \( a \)) and Phase with Min. Voltage (e.g. Phase \( b \)).
Y-Rectifier

Experimental Verification of Output Voltage Balancing

- Symm. Loading  \( P_a = P_b = P_c = 1000 \text{ W} \)
- Asymm. Loading  \( P_a = 730 \text{ W}, P_b = P_c = 1000 \text{ W} \)

\( U_N = 3 \times 230 \text{ V (50 Hz)} \)
\( P_o = 3 \times 1 \text{ kW} \)
\( U_o = 400 \text{ V} \)
\( f_s = 58 \text{ kHz} \)
\( L = 2.8 \text{ mH (on AC-side)} \)
\( C = 660 \mu \text{F} \)

Input Phase Currents, Control Signal \( i_0 \), Output Voltages

- Symm. Loading
- Asymm. Loading

\( i_{N, i} : 1 \text{ A/div} \)
\( V_{DC,i} : 100 \text{ V/div} \)

2 ms/div
△-Rectifier

- Connection of Each Module to All Phases / Rated Power also Available for Phase Loss!
\(
\Delta\text{-Rectifier}
\)

- **Derivation of Equivalent Circuit / Circulating Current Component \(i_0\)**

  \[
  \begin{align*}
  u_{\bar{a}b} &= u_{\bar{a}b}' + u_0 \\
  u_{\bar{b}c} &= u_{\bar{b}c}' + u_0 \\
  u_{\bar{c}a} &= u_{\bar{c}a}' + u_0
  \end{align*}
  \]

  **Def.:**  
  \[
  u_{\bar{a}b}' + u_{\bar{b}c}' + u_{\bar{c}a}' = 0
  \]

- Mains Phase Current Formed by \(u_{\bar{a}b}', u_{\bar{b}c}', u_{\bar{c}a}'\) and \(u_a, u_b, u_c\)

- Circulating Current \(i_0\) Formed by \(u_0\)

  \[
  u_0 = \frac{1}{3}(u_{\bar{a}b} + u_{\bar{b}c} + u_{\bar{c}a})
  \]

- \(u_0\) and/or \(i_0\), which does not appear in \(i_a, i_b\) and \(i_c\), can be maximized by proper synchron. of Module PWM Carrier Signals; Accordingly, Switching Frequency Components of \(u_{\bar{a}b}', u_{\bar{b}c}'\) and \(u_{\bar{c}a}'\) are minimized
**Δ-Rectifier**

- **Y-Equivalent Circuit Describing Mains Current Formation**
  - Equiv. Conc. No-Load Voltage at Terminals $a$, $b$, $c$ (No Circ. Current $i_0$, i.e. No Voltage Drop across $L_Δ$)
    
    \[
    u_{ab} = u_{\bar{a}b} - u_{\bar{b}a},
    \]
    \[
    u_{bc} = u_{\bar{b}c} - u_{\bar{c}b},
    \]
    
  - Equiv. Y-Voltage Syst. should not Contain Zero Sequ. Comp.
    
    \[
    u_{\bar{a}'} + u_{\bar{b}'} + u_{\bar{c}'} = 0 \quad \Rightarrow \quad u_{\bar{b}c}' = u_{\bar{b}'} - (-u_{\bar{a}'} - u_{\bar{b}'}) = u_{\bar{b}'} + 2u_{\bar{b}'} = 2u_{\bar{b}'} + u_{\bar{a}'}
    \]
    
    \[
    u_{\bar{a}'} = \frac{1}{3}(u_{\bar{a}b} - u_{\bar{b}c} - u_{\bar{c}a}),
    \]
    \[
    u_{\bar{b}'} = \frac{1}{3}(u_{\bar{b}c} - u_{\bar{c}b} - u_{\bar{a}b}),
    \]
    \[
    u_{\bar{c}'} = \frac{1}{3}(u_{\bar{c}a} - u_{\bar{a}c} - u_{\bar{b}c})
    \]
    
  - Equiv. Concerning Input Impedance between any Terminals
    
    \[
    Z_{i,\Delta} = Z_{i,Y} \quad \Rightarrow \quad L_\Delta // L_\Delta = \frac{1}{2}L_\Delta = L_Y + L_Y // L_Y = \frac{3}{2}L_Y
    \]
    
    \[
    L_Y = \frac{1}{3}L_\Delta
    \]
- **Δ-Rectifier**

  - **Circulating Current Max. / Minimization of Mains Current Ripple**

  \[ \Delta i_{ab} \]

  \[ \Delta i_{ab} - i_0 \]

  \[ i_0 \]

  - \( U_{LL} = 3 \times 480 \text{ V} \ (50 \text{ Hz}) \)
  - \( P_o = 5 \text{ kW} \)
  - \( U_o = 800 \text{ V} \)
  - \( f_s = 25 \text{ kHz} \)
  - \( L = 2.1 \text{ mH (on AC-Side)} \)

  - For Proper Phase Shift of Module PWM Carrier Signals a Share of the Line-to-Line Current Ripple can be Confined into the Delta Connection.
**Δ-Rectifier**

- **Experimental Results**

\[ U_{LL} = 3 \times 480 \text{ V (50 Hz)} \]
\[ P_o = 5 \text{ kW} \]
\[ U_o = 800 \text{ V} \]
\[ f_s = 25 \text{ kHz} \]
\[ L = 2.1 \text{ mH (on AC-Side)} \]

- **Formation of Input Phase Current**  \( i_a = i_{ab} - i_{ca} \)
- **Circulating Zero Sequence Current**  \( i_0 \)

![Diagram showing currents](image)
Classification of Unidirectional Rectifier Systems

Unidirectional Three-Phase Rectifier Systems

- Passive Systems
  - Single Diode Bridge
    - DC-Side Inductor
    - AC-Side Inductors
    - Passive 3rd Harmonic Injection
  - Multi-Pulse Rect. System
    - (Partial) Transform Isol. or Auto-Transf.-Based
    - AC- or DC-Side Interph. Transformer
    - Passive Pulse Multiplication

- Hybrid Systems
  - Electronic Reactance Based
    - Single Diode Bridge & DC-Side Electron. Ind.
    - Single Diode Bridge & AC-Side Electron. Ind. or Cap.
  - Combination of Diode Rectifier and DC/DC Converter
    - Boost-Type
      - Single Diode Bridge & DC/DC Output Stage
      - Half-Controlled Diode Bridge
      - Multi-Pulse Rect. System (Transf. or Auto-Transf.-Based) with DC/DC Output Stage Empl. AC-Side or DC-Side Ind.
    - Buck-Type
      - Single Diode Bridge & DC/DC Output Stage
      - Half-Controlled Diode Bridge

- Active 3rd Harmonic Injection
  - Active 3rd Harmonic Injection
    - Passive/Hybr. or Active 3rd Harm. Inject. Network
    - Boost- or Buck-Type or Uncontrolled Output
    - Diode Bridge or Multipulse System With Harmonic Inj. (Pulse Multipl.)

- Active PFC Systems
  - Direct Three-Phase Systems
    - Impressed Input Current (Boost-Type)
      - DCM
        - Single-Switch
        - Two-Switch
      - CCM
      - Two-Level Converter
        - Y-Switch
        - Δ-Switch
        - Y-Arrangement With Mains Artificial Star-Point Connection
        - Three-Level Converter (VIENNA Rectifier)
  - Phase-Modular Systems
    - Impressed Input Voltage (Buck-Type)
      - DVM
      - CVM
      - Single-Switch Converter
      - Three-Switch Converter
      - Six-Switch Converter
Single-Switch + Boost-Type DCM Converter Topology

+ Low Complexity / Single Switch
+ No PWM, Constant Duty Cycle Operation
+ No Current Measurement

- High Peak Current Stress
- Low Frequ. Distortion of Mains Currents / Dep. on $U_{pu}/\bar{U}$
- High EMI Filtering Effort

$U_{LL} = 3 \times 400 \text{ V (50Hz)}$
$P_o = 2.5 \text{ kW}$
$U_o = 800 \text{ V}$
$\text{THD}_i = 13.7 \%$

- Improvement of Mains Current Shape by 6th Harmonic Duty Cycle Modulation or Boundary Mode Operation
- Reduction of EMI Filtering Effort by Interleaving
Two Interleaved Single-Switch Boost-Type DCM Converter Stages

- Interleaving Reduces Switching Frequency Input Current Ripple
- For Low Power Only One Unit Could be Operated – Higher Efficiency

- Low Frequency Mains Current Distortion Still Remaining
- Relatively High Implementation Effort
Two-Switch Boost-Type DCM Converter Topology

- Slightly Lower $THD_I$ for same $U_{pn}/\dot{U}_N$ Component as Single-Switch DCM Converter
- Large Switching Frequency CM Output Voltage Comp.
- High Input Capacitor Current Stress

- Artificial Capacitive Neutral Point $N$
- Decoupling of the Phases
- Pros and Cons. as for Single-Switch Converter
- $T_+$ and $T_-$ Could also be Gated Simultaneously

$U_{LL} = 3 \times 400 \text{ V}$
$P_o = 2.5 \text{ kW}$
$U_0 = 700 \text{ V}$
$THD_I = 9 \%$
Classification of Unidirectional Rectifier Systems

- **Passive Systems**
  - Single Diode Bridge
  - Multi-Pulse Rectifier System

- **Hybrid Systems**
  - Electronic Reactance Based
    - Single Diode Bridge & DC-Side Electron. Ind.
    - Single Diode Bridge & AC-Side Electron. Ind. or Cap.
    - Multi-Pulse Rectifier System Employing Electron. Inter-phase Transf.
  - Combination of Diode Rectifier and DC/DC Converter
  - Active 3rd Harmonic Injection
    - Passive/Hybrid or Active 3rd Harm. Inject. Network
    - Boost- or Buck-Type or Uncontrolled Output
    - Diode Bridge or Multipulse System With Harmonic Inj. (Pulse Multipl.)

- **Active PFC Systems**
  - Direct Three-Phase Systems
    - Impressed Input Current (Boost-Type)
      - DCM
      - CCM
    - Impressed Input Voltage (Buck-Type)
      - DCM
      - CCM

- **Phase-Modular Systems**
  - Y-Rectifier
  - Delta-Rectifier
  - 3/2-Phase Scott-Transf. Based

- **Unidirectional Three-Phase Rectifier Systems**
  - Boost-Type
    - Single Diode Bridge & DC/DC Output Stage
    - Half-Controlled Diode Bridge
    - Multi-Pulse Rect. System (Transf. or Auto-Transf.-Based) with DC/DC Output Stage Empl. AC-Side or DC-Side Ind.
  - Buck-Type
    - Single Diode Bridge & DC/DC Output Stage
    - Half-Controlled Diode Bridge

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APEC. 2011
Two-Level CCM Boost-Type PFC Rectifier Systems

• Y-Switch Rectifier
• Δ-Switch Rectifier
**Y-Switch Rectifier**

- Proper Control of Power Transistors Allows Formation of PWM Voltages at $\bar{a}$, $\bar{b}$, $\bar{c}$ and/or Impression of Sinusoidal Mains Current
**Δ-Switch Rectifier**

- Δ-Switch Rectifier Features Lower Conduction Losses Compared to Y-Switch System

- Active Switch Could be Implemented with Six-Switch Power Module
\section*{\textbf{\Delta}-Switch Rectifier}

\begin{itemize}
  \item Equivalent Circuit / Mains Current Control
  \item Reference Voltages, i.e. the Output of the Phase Current Controllers Need to be Transformed into \textbf{\Delta}-Quantities
  \item Mains Currents Controlled in Phase with Mains Voltages $u_a$, $u_b$, $u_c$
  \item Voltage Formation at $a$, $b$, $c$ is Determined by Switching State of $S_{a\overline{b}\overline{a}}$, $S_{b\overline{c}\overline{b}}$, $S_{c\overline{a}\overline{c}}$ and AND Input Current Direction/Magnitude
  \item Always Only Switches Corresponding to Highest and Lowest Line-to-Line Voltage are Pulsed
  \item Switch of Middle Phase Turned Off Continuously
\end{itemize}

\begin{equation}
\begin{align*}
\overline{u}_{a\overline{b}} &= \overline{u}_a - \overline{u}_b \\
\overline{u}_{b\overline{c}} &= \overline{u}_b - \overline{u}_c \\
\overline{u}_{c\overline{a}} &= \overline{u}_c - \overline{u}_a
\end{align*}
\end{equation}
- Switch Rectifier

**Modulation**

\[ U_{LL} = 115 \text{ V (400Hz)} \]
\[ P_0 = 5 \text{ kW} \]
\[ U_0 = 400 \text{ V} \]
\[ f_s = 72 \text{ kHz} \]

Power Density: 2.35 kW/dm³
**Δ-Switch Rectifier**

- **Experimental Analysis**

\[
U_{LL} = 115 \text{ V (400Hz)} \\
P_o = 5 \text{ kW} \\
U_o = 400 \text{ V} \\
f_s = 72 \text{ kHz}
\]

Power Density: 2.35 kW/dm³
Three-Level Boost-Type CCM PFC Rectifier System

• Derivation of Circuit Topologies
Derivation of Three-Level Rectifier Topologies (1)

- Sinusoidal Mains Current Shaping Requires Independent Controllability of the Voltage Formation of the Phases
Derivation of Three-Level Rectifier Topologies (2)

- Three-Level Characteristics
  - Low Input Inductance Req.
  - Low Switching Losses,
  - Low EMI
- Higher Circuit Complexity
- Control of Output Voltage Center Point Required
Three-Level PFC Rectifier Analysis

- Input Voltage Formation
- Modulation / Sinusoidal Input Current Shaping
- Output Center Point Formation
- Control
- Design Considerations
- EMI Filtering
- Digital Control
- Experimental Analysis
Input Voltage Formation

- Voltage Formation

\[ u_{\bar{a}M} = \frac{1 - s_a}{2} \text{sign}(i_a) \frac{U}{2} \]

is Determined by Phase Switching State AND Direction of Phase Current
Semiconductor Blocking Voltage Stress

Blocking Voltage Definition

- $D_{F+}$: Limited to $U_+$ via Parasitic Diode of $T_{a+}$
- $D_{N+}$: Not Dir. Def. by Circuit Structure
- $D_{N-}$: Not Dir. Def. by Circuit Structure
- $D_{F-}$: Limited to $U_-$ via Paras. Diode of $T_{a-}$
- $T_{a+}$: Limited to $U_+$ via $D_{F+}$
- $T_{a-}$: Limited to $U_-$ via $D_{F-}$
**Impression of Input Current Fund. (Ohmic Fund. Mains Behavior)**

\[ \delta = 0.1^\circ \ldots 0.3^\circ \ (50/60 \text{ Hz}) \]
\[ \delta = 1^\circ \ldots 3^\circ \quad (360 \text{ Hz \ldots 800 Hz}) \]

- Difference of Mains Voltage (e.g. \( u_a \)) and Mains Frequency Comp. of Voltage Formed at Rectifier Bridge Input (e.g. \( \bar{u}_a^{'} \))
- Impresses Mains Current (e.g. \( i_a \))
Def. of Modulation Index:

\[ M = \frac{\tilde{U}}{U} \left( 0 \ldots \frac{2}{\sqrt{3}} \right) \]

Zero-Sequence Signal to Achieve Ext. Mod. Range

\[
\begin{align*}
    u_{\bar{a}0} &= u'_a + u_0 \\
    u_{\bar{b}0} &= u'_b + u_0 \\
    u_{\bar{c}0} &= u'_c + u_0 \\
    u_0 &= \frac{1}{3} (u_{\bar{a}0} + u_{\bar{b}0} + u_{\bar{c}0})
\end{align*}
\]

Generation of \( u_0 \), i.e. 3\(^{rd}\) Harmonic Signal
PWM / Formation of $\bar{u}_a^r$, $\bar{u}_b^r$, $\bar{u}_c^r$ / AC-Side Equiv. Circuit (2)

$\bar{u}_a^r$, $\bar{u}_b^r$, $\bar{u}_c^r$

Impression of Mains Current Fundamental in Combination with $u_a$, $u_b$, $u_c$

$u_a^r = u_{aN'} + \bar{u}_a^r + u_{aN'-}^r$
$u_b^r = u_{bN'} + \bar{u}_b^r + u_{bN'-}^r$
$u_c^r = u_{cN'} + \bar{u}_c^r + u_{cN'-}^r$

Note: $u_{NN'} = 0$

$u_{a0} = u_{a}^r + u_0$
$u_{b0} = u_{b}^r + u_0$
$u_{c0} = u_{c}^r + u_0$

$\bar{u}_0$

Low Frequency Zero Sequence Component for Extending the Modulation Range from $M = 0\ldots1$ (Sinusoidal Modulation) to $M = 0\ldots\frac{2}{\sqrt{3}}$

$u_0 = \bar{u}_0 + u_0^-$

$u_{0^-}$

Switching Frequency CM Voltage Fluctuation of the Output $\rightarrow$ Resulting in CM Current and/or CM Filtering Requirement
Time Behavior of the Components of Voltages $u_a, u_b, u_c$

$$i_a = i_a + i_a$$

Graphs showing variations of voltages $u_a, u_b, u_c$ over time $t$ (ms) and current $i_a$.
Local Average Value of Center Point Current

- Derivation of Low-Frequency Component $i_M$ of Center Point Current Assuming a 3$\text{rd}$ Harmonic Component of $u_0$ as Employed for Increasing the Modulation Range

**Assumption:** $i_a > 0$, $i_b < 0$, $i_c < 0$

$m_a = m'_a + m_0 = M_1 \cdot \cos(\omega t) + M_3 \cdot \cos(3\omega t)$

$m_b = m'_b + m_0 = M_1 \cdot \cos\left(\omega t - \frac{2\pi}{3}\right) + M_3 \cdot \cos(3\omega t)$

$m_c = m'_c + m_0 = M_1 \cdot \cos\left(\omega t + \frac{2\pi}{3}\right) + M_3 \cdot \cos(3\omega t)$

$M_1 = \frac{\hat{U}}{2}$

$M_3 = \frac{\hat{U}_0}{2}$

$\alpha_a = 1 - m_a$ (relative on-time of $T_{a\text{+}}$)

$\alpha_b = 1 - m_b$ (relative on-time of $T_{b\text{+}}$)

$\alpha_c = 1 - m_c$ (relative on-time of $T_{c\text{+}}$)

$i_M = \alpha_a \cdot i_a + \alpha_b \cdot i_b + \alpha_c \cdot i_c$

$= (1 - m_a) \cdot i_a + (1 - m_b) \cdot i_b + (1 - m_c) \cdot i_c$

**RMS of $i_M$ minimal for**

$$\frac{M_3}{M_1} \approx \frac{1}{4}$$

- $m_0$, i.e. PWM incl. 3$\text{rd}$ Harm., Reduces $i_M$ and Extends the Modulation Range
*Cond. States within a Pulse Period / Center Point Current Formation*

- Consider e.g. \( i_a > 0, i_b < 0, i_c < 0 \)

- Switching States (100), (011) are Forming Identical Voltages \( u^r_a, u^r_b, u^r_c \) but Inverse Centre Point Currents \( i_M \)

- Control of \( i_M \) by Changing the Partitioning of Total On-Times of (100) and (011)

- Corresponding Switching States and Resulting Currents Paths

\[
\begin{align*}
(000), & \quad i_M = 0 \\
(001), & \quad i_M = i_a \\
(010), & \quad i_M = -i_b \\
(011), & \quad i_M = i_a \\
(111), & \quad i_M = 0 \\
(110), & \quad i_M = i_c \\
(101), & \quad i_M = i_b \\
(100), & \quad i_M = -i_a
\end{align*}
\]
System Control

- Control Structure
- Balancing of the Partial Output Voltages
Control Structure

- Output Voltage Control
- Mains Phase Current Control
- Control of Output Center Point Potential (Balancing of $U_+$, $U_-$)
- Control of $i_a$, $i_b$, $i_c$ Relies on $u_\alpha$, $u_\beta$, $u_\gamma$
- Control of $u_M$ Relies on $\overline{u}_0$ (DC Component)
- No Cross Coupling of both Control Loops
Control of Potential $u_M$ of Output Voltage Center Point

- Assumption: $i_a > 0$, $i_b < 0$, $i_c < 0$

- Control via DC Component of $u_0$, i.e. by Adding $m_0$ to the Phase Modulation Signals i.e. by Inversely Changing the Rel. On-Times of (100) and (011), $\delta_{(100)}$ and $\delta_{(011)}$, without taking Influence on the Total On-Time $\delta_{(100)} + \delta_{(011)}$. 

Control of Output Voltage Center Point Potential $u_M$

- **Assumption:**
  
  $$U_+ = \frac{1}{2}U + \Delta U$$
  $$U_- = \frac{1}{2}U - \Delta U$$

- **Output Voltage Unbalance Results in Increasing On-Time of $T_{a+}$ and Decreasing Off-Times of $T_{b-}$ and $T_{c-}$ so that the Voltages $\bar{u}^a, \bar{u}^b, \bar{u}^c$ are Formed as in the Symmetric Case ($\Delta U = 0$) and/or the Mains Phase Currents Remain at Sinusoidal Shape

- **Resulting $i_M$** Reduces $\Delta U$, i.e. Self Stability Guaranteed

\[\checkmark\]
Admissible Unbalance of Loading of $U_+$ and $U_-$

- System Tolerates Load Unbalance Dependent on the Voltage Transfer Ratio $(U_+ + U_-)/\hat{U}$ and/or the Value of The Modulation Index $M$
Design Guidelines

• Current Stress on the Components
• Transistor Selection
• Output Pre-Charging at Start-up
Current Stress on Power Semiconductors

6-Switch Circuit Topology

\[ I_{DF,avg} = \frac{M}{4} \hat{I}_N \]
\[ I_{DF, rms} = \left( \frac{2M}{3\pi} \right) \hat{I}_N \]
\[ I_{DN,avg} = \frac{1}{\pi} \hat{I}_N \]
\[ I_{DN, rms} = \frac{1}{2} \hat{I}_N \]

\[ \Delta i_{L.pp,max} = \frac{U}{f_s L_N} \sqrt{\frac{3}{4}} M \left( 1 - M \sqrt{\frac{3}{2}} \right) \]

- Output Voltage > \( \sqrt{3} \hat{U}_{\text{max}} \) (typ. 1.2 \( \sqrt{3} \hat{U}_{\text{max}} \)): \( \hat{U}_{\text{max}} \): Ampl. of Max. Mains Phase Voltage
- Required Blocking Capability of All Semiconductors: \( \frac{1}{2} U \)
Current Stress on Power Semiconductors

3-Switch Circuit Topology

\[
I_{DF\text{-avg}} = \frac{M}{4} I_N
\]
\[
I_{DF\text{-rms}} = \sqrt{\frac{2M}{3\pi}} I_N
\]
\[
I_{DN\text{-avg}} = \frac{1}{\pi} I_N
\]
\[
I_{DN\text{-rms}} = \frac{1}{2} I_N
\]

Output Voltage > $\sqrt{3} \hat{U}_{\text{max}}$ (typ. 1.2 \(\sqrt{3} \hat{U}_{\text{max}}\): \(\hat{U}_{\text{max}}\): Ampl. of Max. Mains Phase Voltage

Required Blocking Capability of All Semiconductors: \(\frac{1}{2} U\)
Nonlin. $C_{\text{oss}}$ of Superjunct. MOSFETs Causes Input Curr. Distortion

- Nonlinear Output Capacitance $C_{\text{oss}}$ of MOSFET (CoolMOS) has to be Charged at Turn-off
- Large Turn-Off Delay for Low Currents (e.g. Delay of CoolMOS IPP60R099 (@ $I_{DS} = 1.3\, \text{A}$): 11% of Switching Cycle @ $f_s = 500\, \text{kHz}$)
- Results in PWM Volt. and/or Input Curr. Distortion
Pre-Charging of Output Capacitors / Start-Up Sequence

- Lower Mains Diode $D_{N-}$ is Replaced by Thyristor
- Inrush Current is Limited by $R_{pre}$
- Switches are not Gated During Start-Up
- Start-up Sequence is Required
Digital Control Issues

- Implementation Using a DSP vs. Using an FPGA
- Sampling Strategy
- Controller Requirements
Software Tasks

- Calculation of Controller Outputs
  - Current Controller
  - Voltage Controller
  - Balancing of Output Voltages

- Startup – Sequence

- Observe Error Conditions
  - Over-Voltage at the Output
  - Over-Current
  - Over-Temperature
  - Output Voltage Unbalance
Digital Control Employing a Single DSP

+ Using ADC’s of DSP
+ PWM Modules of DSP for PWM Gen.

- Sequential Calculation
- Limited Calculation Capability

Parallelization of Controller Calculation Required
Implementation Using a Single FPGA

- External ADCs Required
- Calculation Capability Nearly Unlimited
- Example Timing VR1000 ($f_s = 1$ MHz):
**Implementation Using an FPGA vs. a Single DSP**

- **Single DSP Implementation**
  - No External ADCs Required
  - Easy Debugging
  - Implementation using C
  - Limited Calculation Capability
  - Glue Logic can Not be Included

- **FPGA-Based Implementation**
  - Calc. Capability Nearly Unlimited
  - Glue Logic can be Included
  - External ADCs Required
  - Debugging Not Easily Possible
Sampling Strategy / Current Controller

Current Controller

- PI-Type Controller Shows Problems With Integral Part at Current Zero Crossing
- P-Type Controller + Input Voltage Feed Forward Shows Good Results and can be Extended to P+Lag Controller (Improves Performance)

\[ K(s) = K_p \frac{1 + s T_D}{1 + s T_1} \]

Sampling Strategy

- Sampling at the Pulse Period Midpoint (Symmetric) PWM, Direct Sampling of Fundamental
- Single Update or Double Update Possible
- Current Control of All Three Phases has to be Done in 1 Cycle
Output Voltage Controller / Balancing of Partial Output Voltages

Output Voltage Controller

- Generates Conductance $g_e$ for Ref. Value of Current Controller
- Design for No Steady State Deviation
- Needs to be Able to Handle Loss of a Mains Phase (Bandwidth $<< 2f_N$)
- Should show Good Dynamical Behavior at Load-Steps

PI-Type – Controller is a Good Choice

Balancing of the Output Voltages

- Generates Controller Output $u_0 (m_0)$
- Design for No Steady State Deviation
- Bandwidth has to be Set Lower than Three Times Mains Frequency $f_N$ (Bandwidth $<< 3f_N$)
- Should Show Lowest Dynamic of all Control Loops

PI-Type – Controller is a Good Choice
Example of Implementation Using an FPGA (VR250)

FPGA: ECP2 Lattice

- **ADC Interface (Demultiplexer)**
- **Current Controller ($I_c$) (P+Lag, voltage feedback)***
- **DPWM (10 bit)**
- **Voltage Controller (PI-type) ($P^*, g^*, k_v$)**
- **FSM STARTUP**
  - Start-up State Machine
- **Voltage Symmetry Controller (PI-type) ($I_v$)**
- **SYS_CTRL**
  - Generates:
    - Sample Tick
    - PWM_enable
    - PWM_update
- **HW-Monitor**
- **FPGALink**

**CLK generation**
- ADC_Clk: 81.25 MHz
- SYSTick 1 kHz
- RMSTick (50 kHz) 15.3 kHz
- RMSTick (400 kHz) 61 kHz

**System Parameters**
- **Clock (25 MHz)**
- **Input Voltage $V_{in}$**
- **Output Voltage $V_{out}$**

**Additional Notes**
- CHECK Signals
- CalcVN MeasRMS FilterVo
- PLL
  - 125 MHz / 0°
  - 125 MHz / 180°
  - 15.625 MHz / 0°

This diagram illustrates the implementation of a FPGA-based system, detailing various components and their interconnections, including voltage and clock management systems.
EMI Filtering

- DM Filtering
- CM Filtering
**EMI Filtering Concept**

- **DM and CM Filter Stages**
- **Connection of Output Voltage Midpoint $M$ to Artificial Mains Star-Point $N'$**
  - No High-Frequency CM-Voltage at $M$
  - Capacitance of $C_{FB}$ Not Limited by Safety Standards
- **Parasitic Capacitances have to be Considered for CM-Filter Design**
DM Filter Design

- **DM Equivalent Circuit**

- **Required DM Attenuation, e.g. for**
  \( f_s = 1 \text{ MHz} \) (VR1000)

- **DM Filter Structure**
**CM Filter Design**

- **CM Equivalent Circuit**

\[ C_{FB} = 220 \text{ nF} \]

- **Required CM Attenuation**
EMI Filter Structure for VR1000 Rectifier System

- 3 Stage DM Filter
- 2 Filter Stages for CM Filter

- 3 x CM Inductors in Series to Implement Proposed Filter Concept
- Additional CM Filter Stage Required Due to Parasitic Capacitances
Experimental Analysis

- Power Density / Efficiency Pareto Limit
- Experimental Analysis – VR250
Experimental Analysis

- Generation 1 – 4 of VIENNA Rectifier Systems

- Switching Frequency of $f_s = 250$ kHz Offers Good Compromise Concerning Power Density / Weight per Unit Power, Efficiency and Input Current Quality $\text{THD}_i$

<table>
<thead>
<tr>
<th>Frequency ($f_s$)</th>
<th>Power Density ($\rho$)</th>
<th>Weight</th>
</tr>
</thead>
<tbody>
<tr>
<td>50 kHz</td>
<td>3 kW/dm$^3$</td>
<td>3.4 kg</td>
</tr>
<tr>
<td>72 kHz</td>
<td>4.6 kW/dm$^3$</td>
<td></td>
</tr>
<tr>
<td>250 kHz</td>
<td>10 kW/dm$^3$</td>
<td></td>
</tr>
<tr>
<td>1 MHz</td>
<td>14.1 kW/dm$^3$</td>
<td>1.1 kg</td>
</tr>
</tbody>
</table>
Demonstrator – VR250 (1)

- Specifications
  \[ U_{LL} = 3 \times 400 \text{ V} \]
  \[ f_N = 50 \text{ Hz} \ldots 60 \text{ Hz or } 360 \text{ Hz} \ldots 800 \text{ Hz} \]
  \[ P_o = 10 \text{ kW} \]
  \[ U_o = 2 \times 400 \text{ V} \]
  \[ f_s = 250 \text{ kHz} \]

- Characteristics
  \[ \eta = 96.8 \% \]
  \[ \text{THD}_i = 1.6 \% @ 800 \text{ Hz} \]
  \[ 10 \text{ kW/dm3} \]
  \[ 3.3 \text{ kg (≈}3 \text{ kW/kg)} \]

Dimensions: 195 x 120 x 42.7 mm\(^3\)
Demonstrator – VR250 (2)

- **Specifications**

  \[ U_{LL} = 3 \times 400 \text{ V} \]
  \[ f_H = 50 \text{ Hz} \ldots 60 \text{ Hz or } 360 \text{ Hz} \ldots 800 \text{ Hz} \]
  \[ P_o = 10 \text{ kW} \]
  \[ U_o = 2 \times 400 \text{ V} \]
  \[ f_s = 250 \text{ kHz} \]

- **Characteristics**

  \[ \eta = 96.8 \% \]
  \[ \text{THD}_i = 1.6 \% \text{ @ } 800 \text{ Hz} \]
  \[ 10 \text{ kW/dm}^3 \]
  \[ 3.3 \text{ kg (≈3 kW/kg)} \]

Dimensions: 195 x 120 x 42.7 mm³
Mains Behavior @ $f_N = 50$ Hz

$P_0 = 4\text{ kW}$
$U_N = 230\text{ V}$
$f_N = 50\text{ Hz}$
$U_O = 800\text{ V}$
$THD_i = 1.1\%$
Mains Behavior @ $f_N = 400\text{Hz} / 800\text{Hz}$

- $P_O = 10\text{kW}$
- $U_N = 230\text{V}$
- $f_N = 400\text{Hz}$
- $U_O = 800\text{V}$
- $THD_i = 1.4\%$

- $P_O = 10\text{kW}$
- $U_N = 230\text{V}$
- $f_N = 800\text{Hz}$
- $U_O = 800\text{V}$
- $THD_i = 1.6\%$
Demonstrator Performance (VR250)

- Input Current Quality @ $f_N = 800$ Hz

- Efficiency @ $f_N = 800$ Hz
Demonstrator (VR250) Control Behavior

- Mains Phase Loss

- Mains Phase Return
Demonstrator (VR250) EMI Analysis

- Total Emissions
- DM Emissions
- CM Emissions
Coffee Break!
Classification of Unidirectional Rectifier Systems

Unidirectional Three-Phase Rectifier Systems

- Passive Systems
  - Single Diode Bridge
  - Multi-Pulse Rect. System
    - DC-Side Inductor
    - AC-Side Inductors
    - Passive 3rd Harmonic Injection
    - (Partial) Transf. Isol. or Auto-Transf.-Based
    - AC- or DC-Side Interph. Transformer
    - Passive Pulse Multiplication

- Hybrid Systems
  - Electronic Reactance Based
    - Single Diode Bridge & DC-Side Electron. Ind.
    - Single Diode Bridge & AC-Side Electron. Ind. or Cap.
  - Combination of Diode Rectifier and DC/DC Converter
    - Boost-Type
      - Single Diode Bridge & DC/DC Output Stage
      - Half-Controlled Diode Bridge
      - Multi-Pulse Rect. System (Transf. or Auto-Transf.-Based) with DC/DC Output Stage Empl. AC-Side or DC-Side Ind.
    - Buck-Type
      - Single Diode Bridge & DC/DC Output Stage
      - Half-Controlled Diode Bridge

- Active 3rd Harmonic Injection
  - Active 3rd Harmonic Injection
    - Passive/Hybrid or Active 3rd Harm. Inject. Network
    - Boost- or Buck-Type or Uncontrolled Output
    - Diode Bridge or Multipulse System With Harmonic Inj. (Pulse Multipl.)

- Active PFC Systems
  - Direct Three-Phase Systems
  - Impressed Input Current (Boost-Type)
    - DCM
    - CCM
    - Single-Switch
    - Two-Switch
  - Impressed Input Voltage (Buck-Type)
    - DVM
    - CVM
    - Single-Switch Converter
    - Three-Switch Converter
    - Six-Switch Converter
  - Phase-Modular Systems
    - Y-Rectifier
    - Delta-Rectifier
    - 3/2-Phase Scott-Transf. Based
  - Y-Arrangement With Mains Artificial Star-Point Connection
  - Three-Level Converter (VIENNA Rectifier)
Buck-Type CVM PFC Rectifier System

• *Derivation of Circuit Topologies*
Derivation of the Circuit Topology (1)

- Insertion of Switches in Series to the Diodes

+ DC Current Distribution to Phases a, b, c can be Controlled
+ Control of Output Voltage $0 \leq u \leq \frac{3}{2} \hat{U}$

- Pulsating Input Currents / EMI Filtering Requ.
- Relatively High Conduction Losses
Derivation of the Circuit Topology (2)

- Insertion of 4Q-Switches on the AC-Side in Order to Enable Control of the DC Current Distribution to Phases $a$, $b$, $c$
Derivation of the Circuit Topology (3)

- Circuit Extensions

- Internal Filtering of CM Output Voltage Component

- Integration of Boost-Type Output Stage

- Wide Output Voltage Range, i.e. also $\hat{U} > \frac{3}{2} \hat{U}$

- Sinusoidal Mains Current also in Case of Phase Loss

- Circuit Extensions Shown for 3-Switch Topology, but is also Applicable to 6-Switch Topology
Buck-Type PFC Rectifier Analysis

• Modulation
• Input Current Formation
• Output Voltage Formation
• Experimental Analysis
Modulation Scheme

- Consider 60°-Wide Segment of the Mains Period; Suitable Switching States Denominated by \((s_a, s_b, s_c)\)

- Clamping to Phase with Highest Absolute Voltage Value, i.e.
  - Phase \(a\) for \(\omega t \in \left(-\frac{\pi}{6}, \frac{\pi}{6}\right)\),
  - Phase \(c\) for \(\omega t \in \left(\frac{\pi}{6}, \frac{\pi}{2}\right)\) etc.

- Assumption: \(\omega t \in \left(0, \frac{\pi}{6}\right)\)

- Clamping and “Staircase-Shaped” Link Voltage in Order to Minimize the Switching Losses
- Assumption: \( \omega t \in \left( 0, \frac{\pi}{6} \right) \)

- Ohmic Mains Behavior:
  
  \[
  i_a = G^* u_a = (\alpha_b + \alpha_c) \cdot I \\
  i_b = G^* u_b = -\alpha_b \cdot I \\
  i_c = G^* u_c = -\alpha_c \cdot I
  \]

- Example:
  
  \[
  \alpha_b + \alpha_c = \frac{G^* u_a}{I} = \frac{G^* U}{I} \cdot \cos(\omega t) = M \cdot \cos(\omega t)
  \]

  \[
  \alpha_b = -\frac{G^* u_b}{I} = M \cdot \cos \left( \omega t - \frac{2\pi}{3} \right)
  \]

  \[
  M \in (0 ... 1), I \geq \hat{I}^* \\
  \alpha_c = -\frac{G^* u_c}{I} = M \cdot \cos \left( \omega t + \frac{2\pi}{3} \right)
  \]
- Assumption: \( \omega t \in \left(0, \frac{\pi}{6}\right) \)

- Output Voltage Formation:

  \[ \bar{u} = u_{ab} \cdot \alpha_b + u_{ac} \cdot \alpha_c \]

  \[ P_{\text{link}} = P_{\text{input}} \]

  \[ \bar{u} \cdot I = \frac{3}{2} \cdot \hat{U} \cdot \hat{I} \]

  \[ \bar{u} = \frac{3}{2} \cdot \hat{U} \cdot \frac{\hat{I}}{I} = \frac{3}{2} \cdot \hat{U} \cdot M \]

- Output Voltage is Formed by Segments of the Input Line-to-Line Voltages
- Output Voltage Shows Const. Local Average Value
Experimental Results

Ultra-Efficient Demonstrator System

\[ U_{LL} = 3 \times 400 \text{ V (50 Hz)} \]
\[ P_0 = 5 \text{ kW} \]
\[ U_0 = 400 \text{ V} \]
\[ f_s = 18 \text{ kHz} \]
\[ L = 2 \times 0.65 \text{ mH} \]

\[ \eta = 98.8\% \ (\text{Calorimetric Measurement}) \]
Experimental Results

Ultra-Efficient Demonstrator System

\[ U_{LL} = 3 \times 400 \, \text{V} \, (50 \, \text{Hz}) \]
\[ P_0 = 5 \, \text{kW} \]
\[ U_0 = 400 \, \text{V} \]
\[ f_s = 18 \, \text{kHz} \]
\[ L = 2 \times 0.65 \, \text{mH} \]

\[ \eta = 98.8\% \, \text{(Calorimetric Measurement)} \]
Summary of Unidirectional PFC Rectifier Systems

- Block Shaped Input Current Systems
- Sinusoidal Input Current Systems
Block Shaped Input Current Rectifier Systems

Boost-Type

\[ u_a = \dot{U} \cos(\omega t) \]

\[ U > \sqrt{3} \dot{U} \]

0 \rightarrow u_{pn}

Buck-Type

\[ 0 \leq U < \frac{3}{2} \dot{U} \]

0 \rightarrow u_{pn}

Buck+Boost-Type

\[ U \geq 0 \]

0 \rightarrow u_{pn}

- Controlled Output Voltage
- Low Complexity
- High Semicond. Utilization
- Total Power Factor \( \lambda \approx 0.95 \)
- \( \text{THD}_I \approx 30\% \)
Sinusoidal Input Current Rectifier Systems (1)

- **Boost-Type**
  - Controlled Output Voltage
  - Relatively Low Control Complexity
  - Tolerates Mains Phase Loss
  - 2-Level Characteristic
  - Power Semiconductors Stressed with Full Output Voltage

- Controlled Output Voltage
- 3-Level Characteristic
- Tolerates Mains Phase Loss
- Power Semicond. Stressed with Half Output Voltage
- Higher Control Complexity

- Low Current Stress on Power Semicond.
- In Principal No DC-Link Cap. Required
- Control Shows Low Complexity
- Sinusoidal Mains Current Only for Const. Power Load
- Power Semicond. Stressed with Full Output Voltage
- Does Not Tolerate Loss of a Mains Phase
**Sinusoidal Input Current Rectifier Systems (2)**

**Buck-Type**

+ Allows to Generate Low Output Voltages
+ Short Circuit Current Limiting Capability
- Power Semicond. Stressed with LL-Voltages
- AC-Side Filter Capacitors / Fundamental Reactive Power Consumption

**Buck+Boost-Type**

+ See Buck-Type Converter
+ Wide Output Voltage Range
+ Tolerates Mains Phase Loss, i.e. Sinusoidal Mains Current also for 2-Phase Operation
- See Buck-Type Converter (6-Switch Version of Buck Stage Enables Compensation of AC-Side Filter Cap. Reactive Power)
Coffee Break!
Bidirectional PFC Rectifier Systems

- Boost-Type Topologies
- Buck-Type Topologies
Boost-Type Topologies
Classification of Bidirectional Boost-Type Rectifier Systems
Derivation of Two-Level Boost-Type Topologies

- Output Operating Range
Derivation of Three-Level Boost-Type Topologies

- Output Operating Range
Comparison of Two-Level/Three-Level NPC Boost-Type Rectifier Systems

- Two-Level Converter Systems
  + State-of-the-Art Topology for LV Appl.
  + Simple, Robust, and Well-Known
  + Power Modules and Auxiliary Components Available from Several Manufacturers
  - Limited Maximum Switching Frequency
  - Large Volume of Input Inductors

- Two-Level → Three-Level Converter Systems
  + Reduction of Device Blocking Voltage Stress
  + Lower Switching Losses
  + Reduction of Passive Component Volume
  - Higher Conduction Losses
  - Increased Complexity and Implementation Effort
Active Neutral Point Clamped (ANPC) Three-Level Boost-Type System

- Active Distribution of the Switching Losses Possible
- Better Utilization of the Installed Switching Power Devices

- Higher Implementation Effort Compared to NPC Topology
T-Type Three-Level Boost-Type Rectifier System

- Semiconductor Losses for Low Switching Frequencies
  Lower than for NPC Topologies
- Can be Implemented with Standard Six-Pack Module
- Requires Switches for 2 Different Blocking Voltage Levels
Three-Level Flying Capacitor (FC) Boost-Type Rectifier System

+ Lower Number of Components (per Voltage Level)
+ For Three-Level Topology only Two Output Terminals

- Volume of Flying Capacitors
- No Standard Industrial Topology
Three-Level Bridge-Leg Inductor (BLI) Boost-Type Rectifier System

- Lower Number of Components (per Voltage Level)
- For Three-Level Topology only Two Output Terminals

- Additional Volume due to Coupled Inductors
- Semiconductor Blocking Voltage Equal to DC Link Voltage
Pros and Cons of Three-Level vs. Two-Level Boost-Type Rectifier Systems

+ Losses are Distributed over Many Semicond. Devices; More Even Loading of the Chips → Potential for Chip Area Optimization for Pure Rectifier Operation
+ High Efficiency at High Switching Frequency
+ Lower Volume of Passive Components

- More Semiconductors
- More Gate Drive Units
- Increased Complexity
- Capacitor Voltage Balancing Required
- Increased Cost

Moderate Increase of the Component Count with the T-Type Topology

Consideration for 10kVA/400V\textsubscript{ac} Rectifier Operation; Min. Chip Area, $T_{j,\text{max}} = 125^\circ$C

Multi-Level Topologies are Commonly Used for Medium Voltage Applications but Gain Steadily in Importance also for Low-Voltage Renewable Energy Applications
Buck-Type Topologies
Derivation of Unipolar Output Bidirectional Buck-Type Topologies

- Output Operating Range

- System also Features Boost-Type Operation
Derivation of Unipolar Output Bidirectional Buck-Type Topologies

- Output Operating Range
End of Part 1
Passive Rectifier Systems

Hybrid Rectifier Systems (Electronic Reactance Based)


Hybrid Rectifier Systems (Active 3rd Harmonic Injection) (1)


Hybrid Rectifier Systems (Active 3\textsuperscript{rd} Harmonic Injection) (2)


Hybrid Rectifier Systems (Combination of Diode Bridge and DC/DC Converter)


Hybrid Rectifier Systems (Multi-Pulse / Half Controlled Rectifier Systems)


Phase Modular Y-Rectifier (1)


Phase Modular Y-Rectifier (2)


Phase Modular \(\Delta\)-Rectifier


Direct Three-Phase Active PFC Converter (Boost-Type DCM Converters)


Direct Active Three-Phase PFC Rectifier Systems (Two-Level CCM Boost-Type) (1)


Direct Active Three-Phase PFC Rectifier Systems (Two-Level CCM Boost-Type) (2)


Direct Active Three-Phase PFC Rectifier Systems (Three-Level CCM Boost-Type) (1)


Direct Active Three-Phase PFC Rectifier Systems (Three-Level CCM Boost-Type) (2)


Direct Active Three-Phase PFC Rectifier Systems (Three-Level CCM Boost-Type) (3)


Direct Active Three-Phase PFC Rectifier Systems (Three-Level CCM Boost-Type) (4)


Direct Active Three-Phase PFC Rectifier Systems (Design Considerations)


Unidirectional Buck-Type PFC Rectifier Systems


Bidirectional Boost-Type PFC Rectifier Systems (1)

Bidirectional Boost-Type PFC Rectifier Systems (2)


Bidirectional Buck- and Buck-Boost Type PFC Rectifier Systems

Coffee Break!
Part 2
Three-Phase AC-AC PWM Converter Systems
Outline

Basics of AC/DC/AC Converter Systems
- Voltage DC-Link (V-BBC)
- Current DC-Link (I-BBC)

Derivation/Analysis of AC/AC MC Topologies
- Indirect Matrix Converter (IMC)
- Conv. Matrix Converter (CMC)

Comparative Evaluation
- V-BBC vs. CMC/IMC
Classification of Three-Phase AC-AC Converters

- Converters with DC-Link
- Hybrid Converters
- Indirect / Direct Matrix Converters
DC-Link AC-AC Converter Topologies

\[ P = \frac{3}{2} U_1 \cdot I_1 \cos \Phi_1 \]
Symmetric Three-Phase Mains

Phase Voltages
\[ u_a = \hat{U}_1 \cos(\omega_1 t) \]
\[ u_b = \hat{U}_1 \cos(\omega_1 (t - \frac{T}{3})) \]
\[ u_c = \hat{U}_1 \cos(\omega_1 (t + \frac{T}{3})) \]

Phase Currents
\[ i_a = \hat{I}_1 \cos(\omega_1 t - \Phi_1) \]
\[ i_b = \hat{I}_1 \cos(\omega_1 (t - \frac{T}{3}) - \Phi_1) \]
\[ i_c = \hat{I}_1 \cos(\omega_1 (t + \frac{T}{3}) - \Phi_1) \]

Instantaneous Power
\[ p(t) = u_a i_a + u_b i_b + u_c i_c = \frac{P}{3} (1 + \cos 2\omega_1 t) + \frac{Q}{3} \sin 2\omega_1 t + \frac{P}{3} \left(1 + \cos 2\omega_1 \left(t - \frac{T}{3}\right)\right) + \frac{Q}{3} \sin 2\omega_1 \left(t - \frac{T}{3}\right) + \frac{P}{3} \left(1 + \cos 2\omega_1 \left(t + \frac{T}{3}\right)\right) + \frac{Q}{3} \sin 2\omega_1 \left(t + \frac{T}{3}\right) \]

\[ P = \frac{3}{2} \hat{U}_1 \cdot \hat{I}_1 \cos \Phi_1 \]
\[ Q = \frac{3}{2} \hat{U}_1 \cdot \hat{I}_1 \sin \Phi_1 \]

\[ p(t) = \frac{P}{3} (1 + \cos 2\omega_1 t) + \frac{P}{3} \left(1 + \cos 2\omega_1 \left(t - \frac{T}{3}\right)\right) + \frac{P}{3} \left(1 + \cos 2\omega_1 \left(t + \frac{T}{3}\right)\right) = \frac{3P}{3} = P \]
All-SiC JFET I-BBC Prototype

- $P_{out} = 2.9$ kVA
- $f_s = 200$ kHz
- 2.4 kVA / liter (42 W/in$^3$)
- 230 x 80 x 65 mm$^3$
Basic Matrix Converter Topologies

\[ \frac{Q}{3} \left( \sin 2\omega_1 t + \sin 2\omega_1 \left( t - \frac{T}{3} \right) + \sin 2\omega_1 \left( t + \frac{T}{3} \right) \right) \equiv 0 \]
V-BBC

Voltage Space Vectors
Modulation
DC-Link Current
VSI Space Vector Modulation (1)

\[
\bar{u}_{2,j} = \frac{2}{3} \left( u_{A,j} + u_{B,j} + u_{C,j} \right)
\]

\[
u_{0,j} = \frac{1}{3} \left( u_{A,j} + u_{B,j} + u_{C,j} \right)
\]

Output Voltage Reference Value

\[
\bar{u}_2^* = \hat{U}_2^* e^{j \varphi_2} = \hat{U}_2^* e^{j \omega_2^* t}
\]

- Switching with Interlock Delay

\[M_2 = \frac{\hat{U}_2^*}{\hat{U}/2}\]

\[2^3 = 8 \text{ Switching States}\]
VSI Space Vector Modulation (2)

Switching State Sequence

\[ \ldots \quad t_\mu = 0 \quad (n\!n\!n) - (p\!n\!n) - (p\!p\!n) - (p\!p\!p) \quad t_\mu = T_P/2 \quad (p\!p\!p) - (p\!p\!n) - (p\!n\!n) - (n\!n\!n) \quad t_\mu = T_P \quad \ldots \]

Formation of the Output Voltage

\[ \bar{u}_2 = \frac{1}{T_P} \int_0^{T_P} \bar{u}_{2,j} \, dt_\mu = d_{(p\!n\!n)} \cdot \bar{u}_{2,(p\!n\!n)} + d_{(p\!p\!n)} \cdot \bar{u}_{2,(p\!p\!n)} = d_{(p\!n\!n)} \frac{2}{3} U + d_{(p\!p\!n)} \frac{2}{3} U e^{i\pi/3} = \bar{u}_2^* \]

Relative On-times

\[ d_{(p\!p\!n)} = \frac{\sqrt{3}}{2} M_2 \sin \left( \frac{\varphi_{\bar{u}_2^*}}{3} \right) \]

\[ d_{(p\!n\!n)} = \frac{\sqrt{3}}{2} M_2 \sin \left( \frac{\pi}{3} - \varphi_{\bar{u}_2^*} \right) \]
VSI Space Vector Modulation (3)

Freewheeling On-time

\[ d_{(n nn)} + d_{(p pp)} = 1 - (d_{(p pn)} + d_{(p nn)}) \]

Discontinuous Modulation

\[
\begin{align*}
\mu &= \left\{ \begin{array}{ll}
0 & (p nn) - (p pn) - (p pp) \\
T_p / 2 & (p pp) - (p pn) - (p nn) \\
T_p / 2 & (n nn) - (p nn) - (p pn) \\
T_p & \ldots
\end{array} \right.
\end{align*}
\]

Space Vector Orientation

\[
\frac{d_{(p pn)}}{d_{(p nn)}} = \frac{\sin \left( \varphi \hat{u}_2^* \right)}{\sin \left( \frac{\pi}{3} - \varphi \hat{u}_2^* \right)}
\]

Modulation Limit

\[
M_{2,\text{max}} = \frac{\hat{U}_{2,\text{max}}}{U/2} = \frac{2}{\sqrt{3}}
\]
VSI Space Vector Modulation (4)

DC-Link Current Shape

\[ i_j = i_{2,j} \]

\[ i_{(nnn)} = 0 \]
\[ i_{(nnp)} = i_C \]
\[ i_{(npp)} = i_A \]
\[ i_{(ppp)} = 0 \]
\[ i_{(ppn)} = i_B \]
\[ i_{(pnp)} = i_A + i_C = -i_B \]
\[ i_{(pnn)} = i_A + i_B = -i_C \]

Local Average Value

\[ \bar{i} = \frac{1}{T_p} \int_0^{T_p} i_j \, dt_p \]
\[ \bar{i} = -i_C d_{(ppn)} + i_A d_{(pnn)} \]
VSI Space Vector Modulation (5)

Local DC-Link Current Shape

\[ \bar{i} = I = \frac{3}{4} M_2 \hat{I}_2 \cos \Phi_2 \]
VSI DC-Link Current Waveform

Influence of Output Voltage Phase Displacement $\Phi_2$ on DC-Link Current Waveform

$$
\vec{\mathbf{i}} = I = \frac{3}{4} M_2 \hat{I}_2 \cos \Phi_2 \\
M_2 = \frac{2}{\sqrt{3}}
$$
VSI Functional Equivalent Circuit

Voltage Conversion

\[ M_2 = \frac{\hat{U}_2^*}{U/2} \]

\[ u = U \]

\[ \frac{3}{4} \]

\[ \cos \Phi_2 \]

\[ \omega^*_2 \]

Load

\[ \bar{i} = I = \frac{3}{4} M_2 \hat{i}_2 \cos \Phi_2 \]

Current Conversion
I-BBC

Current Space Vectors
Modulation
DC Link Voltage
CSR Commutation & Equivalent Circuit

Forced Commutation

Natural Commutation

Equivalent Circuit

- \(3^2 = 9\) Switching States
- Overlapping Switching
CSR Space Vector Modulation (1)

\[
\bar{i}_k = \frac{2}{3} \left( i_a, k + a i_b, k + a^2 i_c, k \right) \quad a = e^{j2\pi/3}
\]

Input Current Reference Value

\[
\bar{I}_1^* = \hat{I}_1^* e^{j\varphi_1} = \hat{I}_1^* e^{j(\omega_1 t - \Phi_1^*)}
\]

\[
M_1 = \frac{\hat{I}_1^*}{I}
\]

\[
M_{1,\text{max}} = 1
\]
CSR Space Vector Modulation (2)

\[ |\vec{v}_{1,k}| = i_{1,k} = \frac{2}{\sqrt{3}} \cdot I \]

\[ \vec{i}_1 = \frac{1}{T_P} \int_0^{T_P} \vec{i}_{1,k} \, dt \mu = d_{(ac)} \cdot \vec{i}_{1,(ac)} + d_{(ab)} \cdot \vec{i}_{1,(ab)} = \vec{i}_1^* \]

Formation of the Input Current

Relative On-times

\[ d_{(ac)} = M_1 \sin \left( \frac{\pi}{6} + \varphi_{i_1^*} \right) \]

\[ d_{(ab)} = M_1 \sin \left( \frac{\pi}{6} - \varphi_{i_1^*} \right) \]

\[ d_{(aa)} = 1 - (d_{(ac)} + d_{(ab)}) \]

Space Vector Orientation

\[ \varphi_{\vec{u}_1} = \varphi_{\vec{u}_1} - \Phi_1^* \]

\[ \frac{d_{(ac)}}{d_{(ab)}} = \frac{\sin \left( \frac{\pi}{6} + \varphi_{i_1^*} \right)}{\sin \left( \frac{\pi}{6} - \varphi_{i_1^*} \right)} \]
CSR Space Vector Modulation (3)

Switching State Sequence

\[
\begin{align*}
& t_\mu = 0 \quad (ab) - (ac) - (aa) \\
& t_\mu = T_P / 2 \quad (aa) - (ac) - (ab) \\
& t_\mu = T_P \quad (ab) - (ac) - (aa)
\end{align*}
\]

DC-Link Voltage Formation

\[
\begin{align*}
  u_{(ab)} &= u_a - u_b = u_{ab} \\
  u_{(ba)} &= u_b - u_a = -u_{ab} \\
  u_{(bc)} &= u_b - u_c = u_{bc} \\
  u_{(cb)} &= u_c - u_b = -u_{bc} \\
  u_{(ca)} &= u_c - u_a = u_{ca} \\
  u_{(ac)} &= u_a - u_c = -u_{ca} \\
  u_{(aa)} &= u_{(bb)} = u_{(cc)} = 0 \\
  u_k &= \sqrt{3} \cdot u_{1,k} \\
  \bar{u} &= u_{ab}d_{(ab)} + u_{ac}d_{(ac)}
\end{align*}
\]
CSR Space Vector Modulation (4)

Local DC-Link Voltage Shape

\[ \bar{u} = \frac{3}{2} M_1 \tilde{U}_1 \cos \Phi_1^* \]
CSR DC-Link Voltage Waveform

Influence of Input Current Phase Displacement $\Phi_1$ on DC-Link Voltage Waveform

\[ M_1 = \frac{j_1}{I} \]

\[ \bar{u} = \frac{3}{2} M_1 \dot{U}_1 \cos \Phi_1^* \]
CSR Functional Equivalent Circuit

Voltage Conversion

\[ \bar{u} = \frac{3}{2} M_1 U_1 \cos \Phi_1 \]

Current Conversion

\[ M_1 = \frac{i_1^*}{I} \]
Derivation of MC Topologies

*Fundamental Frequency Front End* (F³E)
Classification of Three-Phase AC-AC Converters

- **Converter without DC-Link Capacitor**
$u_{\text{min}} = \frac{3}{2} \hat{U}_1$

$\hat{U}_2^* < \frac{\sqrt{3}}{2} \cdot \hat{U}_1 \approx 0.86 \hat{U}_1$

**P. Ziogas [12]**
**T. Lipo [13, 18, 20]**
**B. Piepenbreier [15]**
Indirect Matrix Converter – IMC

Space Vectors
Modulation
Simulation
Experimental Results
Classification of Three-Phase AC-AC Converters

- Indirect Matrix Converter
IMC Topology Derivation

- Extension of $F^3E$-Topology
- Bidirectional CSR Mains Interface

J. Holtz [16]
K. Shinohara [17]
IMC Properties

- Positive DC-Link Voltage Required!
IMC Voltage and Current Space Vectors
IMC Space Vector Modulation (1)

\[
\vec{u}_1 = \hat{U}_1 e^{j \varphi_{u_1}} = \hat{U}_1 e^{j \omega_1 t} \quad \vec{i}_1 = \hat{I}_1 e^{j \varphi_{i_1}^*},
\]

\[
\vec{u}_2 = \hat{U}_2 e^{j \varphi_{u_2}^*} = \hat{U}_2 e^{j \omega_2 t} \quad \vec{i}_2 = \hat{I}_2 e^{j \varphi_{i_2}^*} = \hat{I}_2 e^{j (\varphi_{u_2}^* - \Phi_2)}
\]
IMC Space Vector Modulation (2)

- Zero Current Commutation
- Zero Voltage Commutation
IMC Zero DC-Link Current Commutation (1)

DC-Link Voltage \[ u = u_{ac} \]
DC-Link Current \[ i = i_A \]
IMC Zero DC-Link Current Commutation (2)

DC-Link Voltage $u = u_{qc}$
DC-Link Current $i = -i_C$

PWM Pattern

120° of Mains Period

DC link Voltage & Current
IMC Zero DC-Link Current Commutation (3)

DC-Link Voltage \( u = u_{ac} \)
DC-Link Current \( i = 0 \)
IMC Zero DC-Link Current Commutation (4)

DC-Link Voltage \( u = u_{ab} \)
DC-Link Current \( i = 0 \)
IMC Zero DC-Link Current Commutation (5)

DC-Link Voltage \( u = u_{qb} \)

DC-Link Current \( i = -i_c \)
IMC Zero DC-Link Current Commutation (6)

DC-Link Voltage \( u = u_{ab} \)
DC-Link Current \( i = i_A \)
IMC Zero DC-Link Current Commutation (7)

Summary

- **Simple and Robust** Modulation Scheme Independent of Commutation Voltage Polarity or Current Flow Direction
- **Negligible Rectifier Stage Switching Losses** Due to Zero Current Commutation
**IMC Space Vector Modulation Calculation**

**Output Voltage Ref. Value**

\[ \vec{u}_2^* = \hat{U}_2^* e^{j\varphi_2^*} = \hat{U}_2^* e^{j\omega_2^* t} \]

**Input Current Ref. Angle**

\[ \vec{i}_1^* = \hat{I}_1 e^{j\varphi_{i_1}^*} \quad \text{and} \quad \varphi_{i_1}^* = \varphi_{u_1}^* - \Phi_1^* \]

**Mains Voltage**

\[ \vec{u}_1 = \hat{U}_1 e^{j\varphi_{u_1}} = \hat{U}_1 e^{j\omega_1 t} \]

**Load Behavior**

\[ \vec{i}_2 = \hat{I}_2 e^{j\varphi_{i_2}} = \hat{I}_2 e^{j(\varphi_{u_2}^* - \Phi_2)} \]

**Assumptions**

\[ \varphi_{u_1} \in \left[ 0, \frac{\pi}{6} \right] \]

\[ \varphi_{u_2}^* \in \left[ 0, \frac{\pi}{3} \right] \]

\[ \varphi_{i_1}^* \in \left[ -\frac{\pi}{6}, \frac{\pi}{6} \right] \]

**PWM Pattern is Specific for each Combination of Input Current and Output Voltage Sectors**
Freewheeling Limited to Output Stage

\[ d_{(ab)} + d_{(ac)} = 1 \]

Input Current Formation

\[ \tilde{i}_a = (d_{(ab)} + d_{(ac)}) \tilde{i} = \tilde{i} \]
\[ \tilde{i}_b = -d_{(ab)} \tilde{i} \]
\[ \tilde{i}_c = -d_{(ac)} \tilde{i} \]

Desired Input Current

\[ \tilde{i}_a = \hat{I}_1 \cos \frac{\varphi^*}{i_1} \]
\[ \tilde{i}_b = \hat{I}_1 \cos \left( \frac{\varphi^*}{i_1} - \frac{2\pi}{3} \right) \]
\[ \tilde{i}_c = \hat{I}_1 \cos \left( \frac{\varphi^*}{i_1} + \frac{2\pi}{3} \right) \]

Resulting Rectifier Stage

Relative On-Times

\[ d_{(ab)} = \frac{\sin \left( \frac{\pi}{6} - \frac{\varphi^*}{i_1} \right)}{\cos \frac{\varphi^*}{i_1}} \]
\[ d_{(ac)} = \frac{\sin \left( \frac{\pi}{6} + \frac{\varphi^*}{i_1} \right)}{\cos \frac{\varphi^*}{i_1}} \]

Absolute On-Times

\[ \tau_{(ab)} = d_{(ab)} \frac{T_p}{2} \]
\[ \tau_{(ac)} = d_{(ac)} \frac{T_p}{2} \]
Mains Voltage

\[ u_a = \bar{U}_1 \cos \left( \varphi \bar{u}_1 \right) \]
\[ u_b = \bar{U}_1 \cos \left( \varphi \bar{u}_1 - \frac{2\pi}{3} \right) \]
\[ u_c = \bar{U}_1 \cos \left( \varphi \bar{u}_1 + \frac{2\pi}{3} \right) \]

Available DC Link Voltage Values

\[ u_{(ab)} = u_{ab} = u_a - u_b = \sqrt{3} \cdot \bar{U}_1 \cos \left( \varphi \bar{u}_1 + \frac{\pi}{6} \right) \]
\[ u_{(ac)} = u_{ac} = u_a - u_c = \sqrt{3} \cdot \bar{U}_1 \cos \left( \varphi \bar{u}_1 - \frac{\pi}{6} \right) \]

Select Identical Duty Cycles of Inverter Switching States (100), (110) in \( \tau_{ac} \) and \( \tau_{ab} \) for Maximum Modulation Range

Switch Conducting the Largest Current is Clamped (over \( \pi/3 \)-wide Interval)
Voltage Space Vectors Related to Active Inverter Switching States

Output Voltage Formation

\[
\bar{u}_2 = \frac{2}{3} u \frac{2/3}{T_p/2} \left( \delta_{(ac)(pnn)} \tau_{(ac)} u_{ac} + \delta_{(ab)(pnn)} \tau_{(ab)} u_{ab} + \delta_{(ac)(ppn)} \tau_{(ac)} u_{ac} e^{j\pi/3} + \delta_{(ab)(ppn)} \tau_{(ab)} u_{ab} e^{j\pi/3} \right)
\]

\[
= \delta_{(pnn)} \frac{2}{3} \left( \frac{\tau_{(ac)}}{T_p/2} u_{ac} + \frac{\tau_{(ab)}}{T_p/2} u_{ab} \right) + \delta_{(ppn)} \frac{2}{3} \left( \frac{\tau_{(ac)}}{T_p/2} u_{ac} + \frac{\tau_{(ab)}}{T_p/2} u_{ab} \right) e^{j\pi/3}
\]

Local DC-link Voltage Average Value

\[
\bar{u} = d_{(ac)} u_{ac} + d_{(ab)} u_{ab}
\]

\[
\bar{u}_2 = \delta_{(pnn)} \frac{2}{3} \bar{u} + \delta_{(ppn)} \frac{2}{3} \bar{u} e^{j\pi/3}
\]

Calculation of the Inverter Active Switching State On-Times can be directly based on \( \bar{u} \)!
DC-Link Voltage Local Average Value

\[ \bar{u} = \frac{3}{2} \cdot \hat{U}_1 \cos \left( \varphi \bar{u}_1 - \varphi^* \right) = \frac{3}{2} \cdot \hat{U}_1 \frac{\cos (\varphi^*)}{\cos (\varphi^*_1)} \]

Minimum of DC-Link Voltage Local Average Value

\[ \bar{u}_{\text{min}} = \frac{3}{2} \hat{U}_1 \cos \Phi^*_1 \]

Resulting IMC Output Voltage Limit

\[ \hat{U}_{2,\text{max}} \leq \frac{\sqrt{3}}{2} \cdot \hat{U}_1 \cos \Phi^*_1 \]

Simulation of DC-Link Voltage and Current Time Behavior
Resulting Inverter Stage
Relative On-Times

\[ \delta_{(ppn)} = \frac{\sqrt{3}}{2} \cdot \frac{\hat{U}_2^*}{\bar{u}/2} \sin \left( \phi \bar{u}_2^* \right) \]

\[ \delta_{(pnn)} = \frac{\sqrt{3}}{2} \cdot \frac{\hat{U}_2^*}{\bar{u}/2} \cos \left( \phi \bar{u}_2^* + \frac{\pi}{6} \right) \]

Resulting Inverter Stage
Absolute On-Times

\[ \tau_{(ac)(pnn)} = \frac{1}{2} T_P d_{(ac)} \delta_{(pnn)} = \frac{1}{2} T_P \frac{2}{\sqrt{3}} \frac{\hat{U}_2^*}{U_1} \frac{1}{\cos \Phi_1^*} \sin \left( \frac{\pi}{6} + \frac{\varphi_{i_1}^*}{\bar{u}_2^*} \right) \cos \left( \phi \bar{u}_2^* + \frac{\pi}{6} \right) \]

\[ \tau_{(ac)(ppn)} = \frac{1}{2} T_P d_{(ac)} \delta_{(ppn)} = \frac{1}{2} T_P \frac{2}{\sqrt{3}} \frac{\hat{U}_2^*}{U_1} \frac{1}{\cos \Phi_1^*} \sin \left( \frac{\pi}{6} + \frac{\varphi_{i_1}^*}{\bar{u}_2^*} \right) \sin \left( \phi \bar{u}_2^* \right) \]
DC-link Voltage Local Average Value

\[ \bar{i}_{(ac)} = \frac{1}{\tau_{(ac)}} (i_A \delta_{(pnn)} \tau_{(ac)} - i_C \delta_{(ppn)} \tau_{(ac)}) = i_A \delta_{(pnn)} - i_C \delta_{(ppn)} \]

\[ \bar{i}_{(ab)} = \frac{1}{\tau_{(ab)}} (i_A \delta_{(pnn)} \tau_{(ab)} - i_C \delta_{(ppn)} \tau_{(ab)}) = i_A \delta_{(pnn)} - i_C \delta_{(ppn)} \]

Equal DC-link Current Local Average Values for Inverter Active Switching States

\[ \bar{i} = \bar{i}_{(ac)} = \bar{i}_{(ab)} = \hat{I}_2 \frac{\hat{U}_2^* \cos \Phi_2}{\hat{U}_1 \cos \Phi_1^*} \cos \frac{\varphi_{*}}{i_1} \]

Local Average Value of Input Current in \( a \)

\[ \bar{i}_a = \bar{i} = \hat{I}_1 \cos \frac{\varphi_{*}}{i_1} \]

Resulting Input Phase Current Amplitude

\[ \hat{I}_1 = \hat{I}_2 \frac{\hat{U}_2^* \cos \Phi_2}{\hat{U}_1 \cos \Phi_1^*} \]

Power Balance of Input and Output Side

\[ \bar{p} = P = \bar{u} \bar{i} = \frac{3}{2} \hat{U}_1 \hat{I}_1 \cos \Phi_1^* = \frac{3}{2} \hat{U}_2^* \hat{I}_2 \cos \Phi_2 \]
IMC Simulation Results
RB-IGBT IMC Experimental Results (1)

- Input RMS voltage: 400V
- Output Power: 6.8 kVA
- Rectifier Switching Frequency: 12.5 kHz
- Inverter Switching Frequency: 25 kHz

Efficiency: 95%

2.9 kW/dm³
48 W/in³
RB-IGBT IMC Experimental Results (2)

\[ U_{12} = 400 \text{V} \]
\[ P_{\text{out}} = 1.5 \text{ kW} \]
\[ f_{\text{out}} = 120 \text{ Hz} \]
\[ f_{S} = 12.5 \text{ kHz} / 25\text{kHz} \]

DC Link Voltage

Input Current

Output Current

100 V/div
5A/div
Alternative Modulation Schemes

► LV and Three-Level Medium Voltage Modulation

High Output Voltage Modulation (HVM)

\[ \hat{U}_2 = 0 \ldots \frac{\sqrt{3}}{2} \cdot \hat{U}_1 \]

Low Output Voltage Modulation (LVM)

\[ \hat{U}_2 = 0 \ldots \frac{1}{2} \cdot \hat{U}_1 \]

Three-Level Modulation

\[ \hat{U}_2 = \frac{1}{2} \ldots \frac{\sqrt{3}}{2} \cdot \hat{U}_1 \]

Weighted Combination of HVM and LVM
Conventional Matrix Converter - CMC

Modulation

Multi-Step Commutation
Classification of Three-Phase AC-AC Converters

- Conventional Matrix Converter
Conventional Matrix Converter – CMC

▶ Quasi Three-Level Characteristic
CMC Classification of Switching States

**Group I**
Freewheeling States

(aaa)  (bbb)  (ccc)

**Group II**
Generating Stationary Output Voltage and Input Current Space Vectors

(eca)  (ecb)  (aab)
(aac)  (bbc)  (bba)
(acc)  (bcc)  (baa)
(cab)  (cbc)  (aba)
(aca)  (bcb)  (bab)

\[
\begin{align*}
 u_{AB} &= 0 \\
 u_{BC} &= 0 \\
 u_{CA} &= 0
\end{align*}
\]

**Group III**
Generating Rotating Space Vectors

(abc)  (cab)  (bca)  \text{ Positive Sequence}
(acb)  (cba)  (bac)  \text{ Negative Sequence}
CMC Stationary Space Vectors

Input Current Space Vectors

Output Voltage Space Vectors
CMC/IMC Relation (1)

Correspondence of Switching States

\[ \vec{u}_{2,(ac)} = \vec{u}_{2,(ac)(pnn)} \]
\[ \vec{i}_{1,(ac)} = \vec{i}_{1,(ac)(pnn)} \]

- Indirect Space Vector Modulation

*P. Ziogas [12]*
*L. Huber / D. Borojevic*
CMC/IMC Relation (2)

Correspondence of Switching States

\[ \mu \in [0, \pi/6] \]

\[ \mu \in [\pi/6, \pi/3] \]

\[ ... | t_\mu = 0 \]

\[ \begin{align*}
(\text{ac})(\text{ppn}) & - (\text{ac})(\text{ppn}) - (\text{ac})(\text{ppp}) \\
& - (\text{ab})(\text{ppp}) - (\text{ab})(\text{ppn}) - (\text{ab})(\text{pnn}) | t_\mu = T_P/2 \\
(\text{ab})(\text{pnn}) & - (\text{ab})(\text{ppn}) - (\text{ab})(\text{ppp}) \\
& - (\text{ac})(\text{ppp}) - (\text{ac})(\text{ppn}) - (\text{ac})(\text{pnn}) | t_\mu = T_P \quad ... \\
\end{align*} \]

\[ \begin{align*}
(\text{acc}) & - (\text{aac}) - \underline{(\text{aaa})} - \underline{(\text{aaa})} - (\text{aab}) - (\text{abb}) | t_\mu = T_P/2 \\
(\text{abb}) & - (\text{aab}) - \underline{(\text{aaa})} - \underline{(\text{aaa})} - (\text{aac}) - (\text{acc}) | t_\mu = T_P \quad ... \\
\end{align*} \]

\[ \begin{align*}
(\text{ac})(\text{ppn}) & - (\text{ac})(\text{ppn}) - (\text{ac})(\text{nnn}) \\
& - (\text{ab})(\text{nnn}) - (\text{ab})(\text{pnn}) - (\text{ab})(\text{pnp}) | t_\mu = T_P/2 \\
(\text{ab})(\text{pnn}) & - (\text{ab})(\text{pnn}) - (\text{ab})(\text{nnn}) \\
& - (\text{ac})(\text{nnn}) - (\text{ac})(\text{pnn}) - (\text{ac})(\text{ppn}) | t_\mu = T_P \quad ... \\
\end{align*} \]

\[ \begin{align*}
(\text{aac}) & - (\text{acc}) - \underline{(\text{ccc})} - \underline{(\text{bbb})} - (\text{abb}) - (\text{aac}) | t_\mu = T_P/2 \\
(\text{aab}) & - (\text{abb}) - \underline{(\text{bbb})} - \underline{(\text{ccc})} - (\text{acc}) - (\text{acc}) | t_\mu = T_P \quad ... \\
\end{align*} \]
CMC Multi-Step Commutation

Example: \( u \)-Dependent Commutation

- Four-Step Commutation
- Two-Step Commutation
4-Step Commutation of CMC (1)

Example: $i$-Dependent Commutation

Constraints

- No Short Circuit of Mains Phases
- No Interruption of Load Current

Assumption: $i > 0$, $u_{ab} < 0$, $aA \rightarrow bA$
4-Step Commutation of CMC (2)

1\textsuperscript{st} Step: Off

Constraints

- No Short Circuit of Mains Phases
- No Interruption of Load Current

Assumption: $i > 0$, $u_{ab} < 0$, \quad aA \rightarrow bA
4-Step Commutation of CMC (3)

1st Step: Off
2nd Step: On

Constraints
- No Short Circuit of Mains Phases
- No Interruption of Load Current

Assumption: \( i > 0, u_{ab} < 0, \quad aA \rightarrow bA \)
4-Step Commutation of CMC (4)

1\textsuperscript{st} Step: Off
2\textsuperscript{nd} Step: On
3\textsuperscript{rd} Step: Off

Constraints

- No Short Circuit of Mains Phases
- No Interruption of Load Current

Assumption: $i > 0, u_{ab} < 0, \ aA \rightarrow bA$
4-Step Commutation of CMC (5)

1\textsuperscript{st} Step: Off
2\textsuperscript{nd} Step: On
3\textsuperscript{rd} Step: Off
4\textsuperscript{th} Step: On

Sequence Depends on Direction of Output Current!

Constraints

- No Short Circuit of Mains Phases
- No Interruption of Load Current

Assumption: $i > 0$, $u_{ab} < 0$, $aA \rightarrow bA$
All-SiC JFET Conventional direct Matrix Converter

- $P_{out} = 3 \text{kVA}, \eta = 93.1\%$ (at 200 kHz)
- $f_{S,\text{nom}} = 144 \text{ kHz} (f_{S,\text{design}} = 200 \text{ kHz})$
- 3 kVA/dm$^3$ (50W/in$^3$) with 1200 V/6 A SiC JFET
- $\approx 8 \text{kVA/dm}^3$ (135W/in$^3$) with 1200 V/20 A SiC JFET
- 273 x 82 x 47mm$^3 = 1.05 \text{ dm}^3$ (64 in$^3$)

Measurements @ $U_{in} = 115 \text{ V RMS, 400 Hz}$

- Input Current 2 A/div
- Output Current 2 A/div
- Input Voltage 200 V/div
Control Properties of AC-AC Converters (1)

Voltage DC-Link B2B Conv. (V-BBC)

- ▶ Boost-Buck-Type Converter
- ▶ Max. Output Voltage can be Maintained during Low Mains Condition

Matrix Converter (CMC/IMC)

- ▶ Buck-Type Converter
- ▶ Maximum Output Voltage is Limited by Actual Input Voltage $\hat{U}_2 = 0.866 \cdot \hat{U}_1$

DC/DC Control Equiv. Circ.
Control Properties of AC-AC Converters (2)

DC-DC Equivalent Circuits

- **IMC**

- **I-BBC**

- **V-BBC**

- **CMC**
Control Properties of AC-AC Converters (3)

- Voltage DC-Link B2B Converter (V-BBC)
- Matrix Converter (CMC / IMC)

- Input Current (in Phase with Input Voltage)
- DC-Link Voltage
- Output Current (Torque and Speed of the Motor)

2 Cascaded Control Loops

- Output Current (Torque and Speed of the Motor)
- Optional: Input Current (Formation of Input Current still Depends on the Impressed Output Current)

2 Cascaded Control Loops
Comparative Evaluation

DC Link Converters
Matrix Converters
Application Areas of Three-Phase PWM Converters

Bidirectional Power Flow

1. Elevators
2. Escalators
3. Cranes
4. Roller Test Benches
5. Automation
6. Production Machinery

Unidirectional Power Flow

1. Renewable Energy
2. MEA
3. Pumps and Compressors
4. Ventilation and AC
5. MEA

60% of Worldwide Ind. Energy Used by Electric Motor Drives! [a]

Motivation

Cost Allocation of VFD Converters

- Control and Gate Drive Circuitry
- Power Semiconductors
- Passive Components
- Cooling System and Mounting

Status Quo ⇒ Motivation

- Holistic Converter System Comparisons are (still) Rarely Found
- Comprehensive Comparisons Involves a Multi-Domain Converter Design
- Voltage-Source-Type Converter Topologies are Widely Used

Focus of the Investigation

- Bidirectional Three-Phase AC/DC/AC and AC/AC Converters
- Low Voltage Drives
- Power Level from 1 kVA to few 10 kVA

[b]: Based on “ECPE Roadmap on Power Electronics, 2008”
Define Application / Mission Profile
- \( M-n \) Operating Range (Continuous / Overload Requirement)
- Torque at Standstill
- Motor Type
- etc.

Compare Required Total Silicon Area (e.g. for \( T_J < 150^\circ C, T_C = 95^\circ C \))
- Guarantee Optimal Partitioning of Si Area between IGBTs and Diodes

- Semiconductor Type, Data
- Thermal Properties
- EMI Specifications
- Converter Type, Motor Type (Losses)
- Modulation Scheme
- etc.

Virtual Converter Evaluation Platform

- Total Si Area – Figure-Of-Merit
- Operating Efficiency
- Average Mission Efficiency
- Total Mission Energy Losses
- EMI Filter Volume
- Costs

Control and Gate Driver Circuitry
Power Semiconductors \( \approx 30\% \)
Passive Components
Cooling System and Mounting
Considered Converter Topologies – V-BBC, I-BBC, IMC, and CMC

With Intermediate Energy Storage

Voltage Source Back-to-Back Converter (V-BBC)

“State-of-the-Art” Converter System

Current Source Back-to-Back Converter (I-BBC)

Without Intermediate Energy Storage

Indirect Matrix Converter (IMC)

Conventional (Direct) Matrix Converter (CMC)

\[ U_{2,\text{max}} = 0.866 U_1 \]
Converter Comparison Overview

- Semiconductor Chip Area ($T_J, T_S$)
- Power Module
- Heat Sink ($T_A, T_S$)
- Gate Driver

Semiconductor and Cooling System Design / Optimization

- Energy Storage
  - Control
  - Power Quality
  - Reactive Power
  - EMI & Filter Topology
  - Loading Limits $\rightarrow$ Lifetime
  - Thermal Properties

Passive Component and EMI Filter Design / Optimization

- Passive Components
- Operating Point
- 4 Topologies
- Converter Topology
- Modulation Scheme
- Semiconductor Losses

Drive System Specs
Comparative Evaluation (1) – Specifications and Operating Points

Main Converter Specifications

- 3 x 400 V / 50 Hz, 15 kVA
  \( f_{sw} = [8 \ldots 72] \text{ kHz} \)
  \( U_{DC} = 700 \text{ V (VSBBC)} \)

- PMSM, Matched to Converter
  \( (L_s \text{ in mH range, } \Phi_2 \approx 0^\circ) \)

- EMI Standard, CISPR 11
  QP Class B (66 dB at 150 kHz)

- Ambient Temperature \( T_A = 50^\circ C \)
  Sink Temperature \( T_S = 95^\circ C \)
  Max. Junction Temperature \( T_{j,max} = 150^\circ C \)
  (for \( T_A = 20^\circ C \Rightarrow T_S = 65^\circ C, T_{j,max} = 20^\circ C \))

Torque Speed Plane

- OP1/OP5: Nominal Motor/Generator Operation (90% \( U_{2,max} \))
- OP2/OP4: Motor/Generator Operation for \( f_2 = f_1 \)
- OP3: Motor Operation at Stand-still \( f_2 = 0 \)

\[ \begin{align*}
\text{Torque} & \sim I_2 \\
\text{Speed} & \sim f_2 \\
\end{align*} \]
Comparative Evaluation (2) – Semicond. Area Based Comparison

VLBBC, OP1
\(A_{\text{Chip}} = 5.0 \, \text{cm}^2\)
\(\eta_{\text{OP1}} = 95.5\%\)

CLBBC, OP1
\(A_{\text{Chip}} = 4.4 \, \text{cm}^2\)
\(\eta_{\text{OP1}} = 94.2\%\)

VLBBC, OP5
\(A_{\text{Chip}} = 7.9 \, \text{cm}^2\)
\(\eta_{\text{OP5}} = 95.6\%\)

CLBBC, OP5
\(A_{\text{Chip}} = 6.1 \, \text{cm}^2\)
\(\eta_{\text{OP5}} = 94.2\%\)

IMC, OP3
\(A_{\text{Chip}} = 5.0 \, \text{cm}^2\)
\(\eta_{\text{OP3}} = 95.6\%\)

IMC, OP5
\(A_{\text{Chip}} = 4.4 \, \text{cm}^2\)
\(\eta_{\text{OP5}} = 94.2\%\)

VLBBC, OP1&5
\(A_{\text{Chip}} = 5.9 \, \text{cm}^2\)
\(\eta_{\text{OP5}} = 96.8\%\)

IMC, OP1&5
\(A_{\text{Chip}} = 5.9 \, \text{cm}^2\)
\(\eta_{\text{OP5}} = 95.6\%\)

Minimum Chip Area Required to Fulfill the Junction Temperature Limit \(T_{j,\text{max}} (150^\circ \text{C})\)

<table>
<thead>
<tr>
<th>Technology</th>
<th>(A_{\text{Chip}}) (cm(^2))</th>
<th>(\eta) (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>VLBBC, OP1</td>
<td>5.0</td>
<td>95.5</td>
</tr>
<tr>
<td>CLBBC, OP1</td>
<td>4.4</td>
<td>94.2</td>
</tr>
<tr>
<td>VLBBC, OP5</td>
<td>7.9</td>
<td>95.6</td>
</tr>
<tr>
<td>CLBBC, OP5</td>
<td>6.1</td>
<td>94.2</td>
</tr>
<tr>
<td>IMC, OP3</td>
<td>5.0</td>
<td>95.6</td>
</tr>
<tr>
<td>IMC, OP5</td>
<td>4.4</td>
<td>94.2</td>
</tr>
</tbody>
</table>

- Transistor and diode chip areas
- Power module size
- Cooling system requirements
- Efficiency
- Costs, etc.
Semiconductor and Cooling System Modeling

Semiconductor Database

- 1200 V Si IGBT4 and EmCon4 Diodes (Infineon)
- 1200 V normally-on SiC JFET (SiCED)

Component Level

- Losses as $f (A_{\text{chip}}, I, U, \text{and } T)$

System Level

- Transient Thermal Impedance
- Scaling of Chip Area
- Heat Spreading

Simulation with ICEPAK and GECKO

Cooling Performance
Comp. Evaluation (3) – Semiconductor Chip Areas (OP1 & OP5)

1200 V Si IGBT4 and EmCon4 Diodes

- Conduction Losses
- Switching Losses

Resulting Sensitivities

1200 V Normally-On SiC JFETs (SiCED)

Conduction Losses

Switching Losses
Comparative Evaluation (4) – Torque Envelope for Equal $A_{\text{chip}}$

- For OP1 ($P_{2N} = 15$ kVA) and OP3 (Stand-Still)

8 kHz: $A_{\text{chip}} \approx 6$ cm$^2$, Referenced to IMC

32 kHz: Available Chip Area $A_{\text{chip}} \approx 6$ cm$^2$

Note: Design at Thermal Limit – A More Conservative Design would be Applied for a Product!
Verification by Electro-Thermal Simulation Shown for IMC

Junction Temperatures OP1

- Suggested Algorithm to Optimally Select the Semiconductor Chip Area Matches well at OP1 and OP3

Evaluated for OP1 @ 8 kHz

Torque at OP1 and OP3

- Suggested Algorithm allows for Accurate Torque Estimation at OP1 and OP3
- Torque Limit Line Requires a Thermal Impedance Model of the Module (R-C Network)
Passive Component and EMI Input Filter Modeling

**Component Level**

<table>
<thead>
<tr>
<th>Component</th>
<th>Unit</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>C</td>
<td>μF</td>
<td>100</td>
</tr>
<tr>
<td>L</td>
<td>μH</td>
<td>100</td>
</tr>
</tbody>
</table>

**System Level**

- CISPR 11 (Compliant to IEC/EN) EMI Standard for CE
- Filter Design Margin
  - DM Design Margin: 6 dB
  - CM Design Margin: 8-10 dB

**Design Criteria and Constraints**

- Ripple-Based ($C_{\text{inp}}, C_{\text{out}}, L_b$)
- Reactive Power ($L_{\text{CM}}$)
- Control-Based ($C_{\text{DC}}, L_{\text{DC}}$)
- Energy-Based ($C_{\text{DC}}, L_{\text{DC}}$)
Comparative Evaluation (5) – Attenuation, Volume of Passives

Volume of Passive Components

- V-BBC Requ. 15 dB More Atten.
Comparative Evaluation (6) – Total Efficiency and Volume

Efficiency vs. Switching Frequency

- V-BBC: Local Optimum at 35 kHz for SiC JFETs
- MC: Significant Volume Reduction

Volume vs. Switching Frequency
Multi-Domain Simulation Software
GeckoCIRCUITS

Input
Topology / Device Models / Control Circuit / 3D-Geometry / Materials

GeckoHEAT

3D-Thermal FEM Solver
Thermal Impedance Matrix
HF Magnetics Design Toolbox

Fast Circuit Simulator

3D-Electromagn. Parasitics Extraction
Reduced Order Impedance Matrix
EMC Filter Design Toolbox

Heatsink Design Toolbox

Reliability Analysis Toolbox

Post Processing
Design Metrics, Sensitivity Calculation, Optimization

Device & Material Database
Control Toolbox
Optimization Toolbox

GeckoEMC

3D-Electromagn. Parasitics Extraction
Reduced Order Impedance Matrix
EMC Filter Design Toolbox

Heatsink Design Toolbox

Reliability Analysis Toolbox

Post Processing
Design Metrics, Sensitivity Calculation, Optimization

Device & Material Database
Control Toolbox
Optimization Toolbox
Overview of Gecko-Software Demonstration

- **Gecko-CIRCUITs: Basic Functionality**

- **Indirect Matrix Converter (IMC)**
  - IMC Simulation with Controlled AC Machine
  - Specify Semiconductor Characteristics
  - Simulate Semiconductor Junction Temperature
  - etc.

- **Gecko EMC: Basic Functionality**
Further Information Regarding Gecko-Research

Power Electronics Simulation - Gecko Research

- Specialized Software to meet demands of Power Electronics Engineers
- Easy-to-use
- Three tools working together: GeckoCIRCUITS, GeckoEMC, GeckoHEAT
- Multi-Domain approach and Optimization
- Coupled Circuit-, Thermal-, and Electromagnetic Simulation

Free Trial Version of GeckoCIRCUITS
- Online Simulator in Applet-Mode
- No installation required!

Power Electronic Converter Optimization

Let’s assume you want to build a single-phase PFC rectifier with 230V input voltage, 400V output voltage and 3.2kW output power. You can optimize this rectifier for highest efficiency or for highest power density or for minimum cost or ...

www.gecko-research.com
Overview of AC-AC Converters

AC/AC-Conversion for Highly Compact Drives - What Options Do I Have?

For operating a Permanent Magnet Synchronous Machine (PMSM), which allows a highly compact design, you have to supply three-phase voltage with controllable output frequency and controllable voltage amplitude. There are many different alternatives for the AC/AC converter. Here you will learn all options.

- Part I - An Overview of AC/AC-Converter Topologies
- Part II - How Can I Compare Topologies?
- Part III - Semiconductor Loss Calculation Demystified
- Part IV - Do You Know the Junction Temperatures of Your Design? (coming soon)
Gecko-Research Application Notes (2)

Useful Hints for e.g. How to Implement Sector Detection for SV Modulation

► JAVA Code Block

- Integration of Complex Control Code; Enhances Overview and Transparency
- Code can Virtually be Copied to DSP C-Code Generator (Minor Syntax Adaptations)
**Power Electronics Converter Optimization**

**Goal: Optimization Toolbox**

- **Guided Step-by-Step Converter Design Procedure to Enable Optimal Utilization of Technological Base and Optimal Matching between Design Specifications and Final Performance**
Conclusions
Hype Cycle of Technologies

-Gartner Group

2000
- Sparse Matrix Converter
- Three-Level Matrix Converter

1995
- Reverse Blocking IGBTs
- Handling of Unbalanced Mains

1990
- Multi-Step Commutation
- Indirect Space Vector Modulation
- Indirect Matrix Converter

1970’s
- Invention of Matrix Converter Topology

2005 –
- Hybrid Matrix Converter
- More Complicated Topologies
- Refinements
- Holistic Comparisons [51-54]

Through of Disillusionment
Conclusions (1)

► **MC is NOT an All-SiC Solution**

- *Industry Engineers Missing Experience*
- *86% Voltage Limit / Application of Specific Motors / Silicon Area*
- *Limited Fault Tolerance*
- *Braking in Case of Mains Failure*
- *Costs and Complexity Challenge*
- *Voltage DC Link Converter could be Implemented with Foil Capacitors*

► **MC does NOT offer a Specific Advantage without Drawback**

► **EMI Filter**
► **Clamp Circuit**
Conclusions (2)

► Research MUST Address Comprehensive System Evaluations
  - MC Promising for High Switching Frequency
  - Consider Specific Application Areas
  - Consider Life Cycle Costs
  - etc.

► V-BBC is a Tough Competitor

► F³E Might Offer a Good Compromise

► Most Advantageous Converter Concept Depends on Application and on whether a CUSTOM Drive Design is Possible

► Integration of Multiple Functions (as for MC) Nearly ALWAYS Requires a Trade-off
End of Part 2
Thank You!
AC-AC Converter Systems (1)

AC-AC Converter Systems (2)


AC-AC Converter Systems (3)


AC-AC Converter Systems (5)


AC-AC Converter Systems (6)


Johann W. Kolar (F’10) received his Ph.D. degree (summa cum laude / promotio sub auspiciis praesidentis rei publicae) from the University of Technology Vienna, Austria. Since 1984 he has been working as an independent international consultant in close collaboration with the University of Technology Vienna, in the fields of power electronics, industrial electronics and high performance drives. He has proposed numerous novel PWM converter topologies, and modulation and control concepts, e.g., the VIENNA Rectifier and the Three-Phase AC-AC Sparse Matrix Converter. Dr. Kolar has published over 350 scientific papers in international journals and conference proceedings and has filed 75 patents. He was appointed Professor and Head of the Power Electronic Systems Laboratory at the Swiss Federal Institute of Technology (ETH) Zurich on Feb. 1, 2001.

The focus of his current research is on AC-AC and AC-DC converter topologies with low effects on the mains, e.g. for power supply of data centers, More-Electric-Aircraft and distributed renewable energy systems. Further main areas of research are the realization of ultra-compact and ultra-efficient converter modules employing latest power semiconductor technology (SiC), novel concepts for cooling and EMI filtering, multi-domain/multi-scale modeling / simulation and multi-objective optimization, physical model based lifetime prediction, pulsed power, bearingless motors, and Power MEMS.

He received the Best Transactions Paper Award of the IEEE Industrial Electronics Society in 2005, the Best Paper Award of the ICPE in 2007, the 1st Prize Paper Award of the IEEE IAS IPCC in 2008, and the IEEE IECN Best Paper Award of the IES PETC in 2009. He also received an Erskine Fellowship from the University of Canterbury, New Zealand, in 2003. He initiated and/or is the founder / co-founder of 4 Spin-off Companies targeting ultra high speed drives, multi-domain/level simulation, ultra-compact/efficient converter systems and pulsed power/electronic energy processing. In 2006, the European Power Supplies Manufacturers Association (EPSMA) awarded the Power Electronics Systems Laboratory of ETH Zurich as the leading academic research institution in Power Electronics in Europe.

Dr. Kolar is a Fellow of the IEEE and a Member of the IEEJ and of International Steering Committees and Technical Program Committees of numerous international conferences in the field (e.g. Director of the Power Quality Branch of the International Conference on Power Conversion and Intelligent Motion). He is the founding Chairman of the IEEE PELS Austria and Switzerland Chapter and Chairman of the Education Chapter of the EPE Association. From 1997 through 2000 he has been serving as an Associate Editor of the IEEE Transactions on Industrial Electronics and since 2001 as an Associate Editor of the IEEE Transactions on Power Electronics. Since 2002 he also is an Associate Editor of the Journal of Power Electronics of the Korean Institute of Power Electronics and a member of the Editorial Advisory Board of the IEEJ Transactions on Electrical and Electronic Engineering.
**Michael Hartmann** (M’09) was born in Feldkirch, Austria, on May 26, 1978. After he finished the HTL-Rankweil (Telecommunications), he started to work at Omicron Electronics in Klaus (Austria) as a hardware development engineer. There, his work was focused on measurements techniques for power system testing.

In October 2001, he began to study electrical engineering at the University of Technology Vienna, Austria. His diploma thesis deals with the design and implementation of a multi-cell switch mode power amplifier with zero-voltage switching DC-links employing a digital modulator. He received his M.Sc. degree with honors in November 2006, and he has been a Ph.D. student at the Power Electronic Systems Laboratory, ETH Zürich, since March 2007.

**Thomas Friedli** (M’09) received his M.Sc. degree in electrical engineering and information technology (with distinction) and his Ph.D. from the Swiss Federal Institute of Technology (ETH) Zürich, in 2005 and 2010, respectively.

From 2003 to 2004 he worked as a trainee for Power-One in the R&D centre for telecom power supplies. His Ph.D. research from 2006 to 2009 involved the further development of current source and matrix converter topologies in collaboration with industry using silicon carbide JFETs and diodes and a comparative evaluation of three-phase ac-ac converter systems.

He received the 1st Prize Paper Award of the IEEE IAS IPCC in 2008 and the IEEE IAS Transactions Prize Paper Award in 2009.